United Electronic Industries

The High-Performance Alternative

DNR-12-1G RACKtangle™ and DNR-6-1G HalfRACK™ Data Acquisition Systems User Manual

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Chapter 1 Introduction

This document describes the features, performance specifications, and operating functions of the DNR-12-1G *RACKtangle ™* and the DNR-6-1G *HalfRACK ™* data acquisition systems. Both systems are identical except for the size of the enclosure and the number of IO modules. Both are designed for use with an Ethernet Gigabit 1000 Base-T communication network.

1.1 Organization of Manual

This DNR-X-1G User Manual, which describes both types of systems, is organized as follows:

- **Chapter 1 – Introduction**
  This chapter.describes the organization of the document and the conventions used throughout the manual.
- **Chapter 2 – DNR-12-1G *RACKtangle*™ System**
  This chapter provides an overview of a DNR-12-1G system, component modules, features, accessories, and a list of all items you need for initial operation.
- **Chapter 3 – DNR-6-1G *HalfRACK*™ System**
  This chapter provides an overview of a DNR-6-1G system, component modules, features, and accessories. It is essentially the same as the DNR-12-1G system except for enclosure size and number and arrangement of modules.
- **Chapter 4 – Installation and Configuration.**
  This chapter summarizes the recommended procedures for installing, configuring, starting up, and troubleshooting a DNR-X-1G system.
- **Chapter 5 – PowerDNA Explorer for the DNR-X-1G**
  This chapter provides a general description of the menus and screens of PowerDNA Explorer when used with a DNR-X-1G system.
- **Chapter 6 – The DNR-CPU-1000Core Module (CPU/NIC)**
  This chapter describes the DNR-CPU-1000 module, which contains a PowerPPC CPU and a GigE Network Interface Module.
- **Chapter 7 – Programming Board-specific Functions**
  This chapter describes tools and facilities used for programming board-specific functions.
- **Appendix A – Configuring Additional Ethernet Cards**
  This appendix describes procedures for installing and configuring additional Ethernet cards for use with various popular operating systems.
- **Appendix B – Field Replacement of Fuses**
  This appendix describes procedures for replacing fuses in the field.
- **Index**
  This is an alphabetical listing of topics covered in the manual, identified by page number.

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Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done, or reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text you should enter verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Before plugging any I/O connector into the Cube or Board, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNA *RACKtangle* ™ rack mounted system, whichever is applicable.

Throughout this manual, the term “DNR-X-1G” refers to both DNR-12-1G and DNR-6-1G types of systems. The DNR-12 can accept up to 12 IO modules and the DNR-6-1G can accept up to 6 IO modules. The two models are identical in all other respects.

Chapter 2 The DNR-12-1G RACKtangle System

2.1 PowerDNR DNR-12-1G System

The UEI PowerDNR DNR-12-1G *RACKtangle ™* product is a rack-mounted version of the popular PowerDNA Cube Ethernet-based Data Acquisition System. The DNR-12-1G houses a PowerDNA data acquisition system in a rack enclosure accessible from the front of the rack. Multiple DNR-12-1G systems may be mounted in a single rack. All standard PowerDNA I/O boards are also available in PowerDNR versions for use in DNR-12-1G systems.

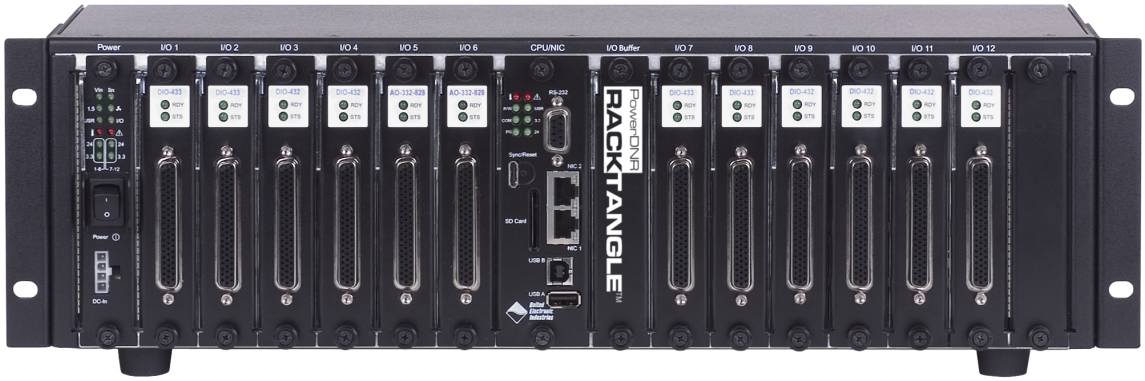

Figure 2-1. Typical PowerDNR DNR-12-1G RACKtangle ™ System

As illustrated in **Figure 2-4** on page 7 and **Figure 2-9** on page 12, a standard PowerDNR rack system consists of the following modules:

- One or more DNR-12-ENCL rack mounted Enclosures
- DNR-POWER-DC Power Module (one for each enclosure)
- DNR-CPU-1000 Module (Freescale MPC8347 CPU and 1-GB Ethernet 1000 Base-T Network Interface Module — one for each enclosure)
- DNR-BUFFER Board Module (one for each enclosure)
- DNR-IO-FILLER panels (one for each unused I/O slot)
  Note: These slot covers are optional and not included in the price of the rack.
- DNR-PSU-24-100 100-Watt, 120/230 VAC to +24VDC External Power Supply (one for each enclosure) with cable and Molex connector for plug-in to the DNR-POWER-DC Module front panel.

To configure a complete data acquisition system, insert up to 12 DNR I/O modules into each PowerDNR rack enclosure, which may be specified in any combination of the following types:

- DNR-AI-201, -202, 205, 207, -208, -211, -225
- DNR-AO-308, -308-350, -308-353, -308-420, -332,
- DNR-DIO-401, -402, -403, 404, -405, 406, -416, -432, -433, -448
- DNR-CT-601, DNR-QUAD-604
- DNR-SL-501, DNR-CAN-503

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- DNR-429-566, DNR-429-512
- DNR-GPS
- Any future additions to the PowerDNR I/O module product line

Note: Refer to www.ueidaq.com for a description of each I/O module.

All standard PowerDNA accessories are also available for use in a PowerDNR rack-mount system.

NOTE: UEIPAC, UEISIM, and UEIModbus deployments are now available for use with DNR-12 RACKtangle systems, with the following model names:

- UEIPAC — UEIPAC 1200R
- UEISIM — UEISIM 1200R
- UEIModbus — UEIModbus 1200R

2.2 Specifications

Figure 2-2 lists the technical specifications of the DNR-12-1G PowerDNR system.

Standard Interfaces	
To Host Computer	Two independent 1000Base-T Gigabit Ethernet ports via RJ-45 connector
Distance from host	100 meters, max
Other Interfaces	One USB 2.0 controller port, One USB 2.0 slave port.
Config/General	RS-232, 9-pin "D"
Sync	Custom cable to sync multiple racks
I/O Slots Available	
DNR-12-1G	12 slots
Data transfer and communications rates	
Ethernet data transfer rate	20 megabytes per second
Analog data transfer rate	up to 6 megasample per sec (16-bit samples)
DMAP I/O mode	update 1000 I/O channels (analog and/or digital) in less than 1 millisecond, guaranteed
Processor	
CPU	Freescale 8347, 400 MHz, 32-bit
Memory	128 MB (not including on-board Flash)
Status LEDs	Power supplies within spec, One second system heart-beat, Attention, Read/Write, Power, Communications Active
Environmental	
Temp (operating)	Tested to -40 °C to 70 °C
Temp (storage)	-40 °C to 100 °C
Humidity	0 to 95%, non-condensing
Vibration	
(IEC 60068-2-64)	10-500 Hz, 3 g (rms), Broad-band random
(IEC 60068-2-6)	10-500 Hz, 3 g, Sinusoidal
Shock	
(IEC 60068-2-27)	50 g, 3 ms half sine, 18 shocks at 6 orientations; 50 g, 11 ms half sine, 18 shocks at 6 orientations
Physical Dimensions	
DNR-12 series	5.25" x 6.2" x 17.5" (3U in a 19" rack)
Power Requirements	
Voltage	9 - 36 VDC (AC adaptor included)
Fuse	Internal 10 A
Power Dissipation	13 W at 24 VDC (not including I/O boards)
Power Monitoring	
I/O board power	All internal power supplies monitored to ±1% accuracy. All PS voltages may be read by host. LED annunciators indicate out of range
Input current	Monitored by host, LED indicates overcurrent
Input voltage	Monitored by host, LED indicates out of range

Figure 2-2. DNR-12-1G Technical Specifications

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2.3 Key Features

The following table is a list of key features of a DNR-12-1G PowerDNR system.

Easy to Configure and Deploy

- Over 25 different I/O boards available
- Over 5 quadrillion possible configurations
- Built-in signal conditioning
- Gigabit Ethernet based
- Bracket kit for mounting to wall or in 19" racks
- Industrial quality rubber feet for solid table-top mounting
- Passive backplane ensures extremely low MTTR
- Standard "Off-the-shelf" products and delivery

True Real-time Performance

- 1 msec updates guaranteed with 1000 I/O
- Up to 6 million samples per second
- Use QNX, RTX, RT Linux, RTAI Linux, LabVIEW RT

Flexible Connectivity

- 1000Base-T with Cat-5 cable
- 10/100Base-FX Fiber interface available (see DNR-FPPC family)
- Supports WIFI / GSM / Cell networks
- Built-in USB 2.0 slave and controller ports

Compact Size:

- 5.25" x 6.2" x 17.5"
- 300 analog inputs per rack
- 384 analog outputs per rack
- 576 digital I/O bits per rack
- 96 counter/quadrature channels per rack
- 144 ARINC-429 channels per rack
- 48 RS-232/422/485 ports per rack

Low Power:

- Less than 50 watts per typical rack (including I/O)*
- AC, 9-36 VDC or battery powered.

Stand alone and Data Logger Modes

- Upgradable to UEILogger 1200R
- Upgradable to UEIPAC 1200R
- Upgradable to UEIModbus 1200R

Rugged and Industrial:

- Solid Aluminum construction
- Operation tested from -40°C to +70°C
- Vibration tested to TBD g, (operating)
- Shock tested to TBD g (operating)
- All I/O isolated from rack and host PC.
- Operation to TBD feet

Outstanding Software Support

- Windows, Linux, RT Linux, Windows RT, RTX and QNX operating systems
- VB, VB .NET, C, C#, C++, J#
- MATLAB, LabVIEW, LabVIEW RT, DASYLab, OPC, ActiveX

*Varies with layer types, Refer to layer datasheets.

Figure 2-3. DNR-12-1G PowerDNR Product Features

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2.4 DNR-12-1G PowerDNR System Enclosure

Because a major design goal of the DNR product line is to allow easy configuration and updates in the field, each DNR-12-1G enclosure contains a DNR-POWER-DC Power Module with status indicating LEDs and a local ON/OFF switch — and each I/O module is provided with a mechanical lever (see **Figure 2-6** on page 9) for quick ejection and insertion of the board. In addition, each DNR-12-1G system enclosure also contains its own GigE CPU and two Network Interface Control (NIC) modules, one for controlling up to 12 I/O modules mounted in the enclosure, and another for diagnostics functions. The module-specific I/O boards are functionally identical to the corresponding modules for the PowerDNA Cube.The only differences between the two types relate to the mounting arrangements.

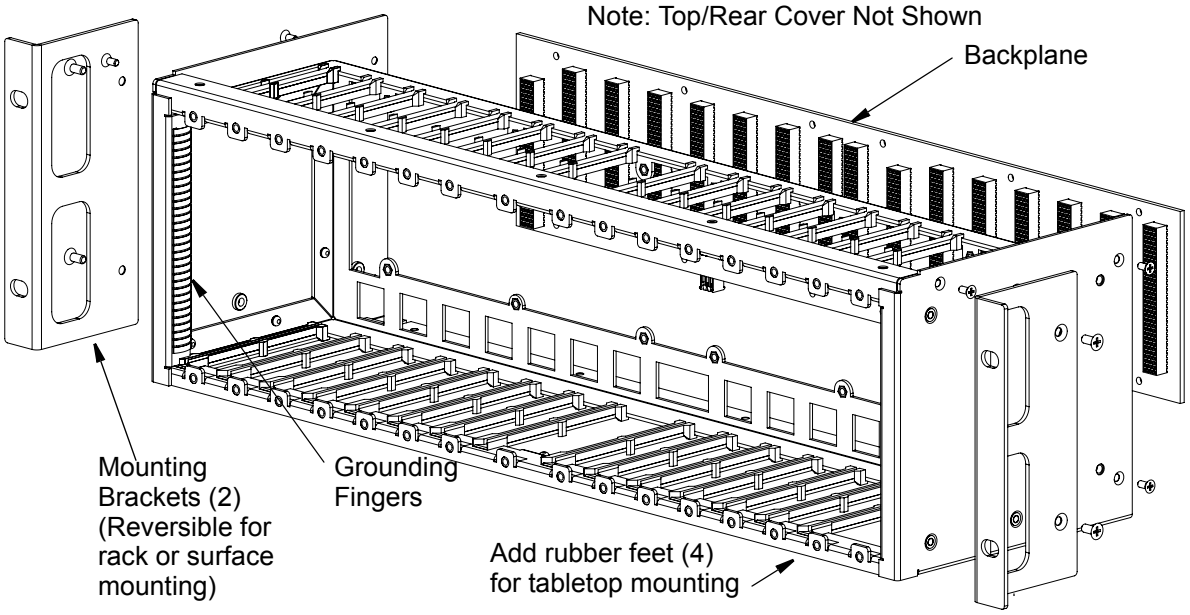
Note: Top/Rear Cover Not Shown
Backplane
Mounting Brackets (2) (Reversible for rack or surface mounting)
Grounding Fingers
Add rubber feet (4) for tabletop mounting

Figure 2-4. Typical PowerDNR DNR-12-ENCL Enclosure (Exploded View)

As shown in **Figure 2-4** and **Figure 2-9**, the PowerDNR DNR-12 enclosure is designed to house the following items:

- One isolated DNR-POWER-DC DC/DC Power Module/Power Monitor with status indicating LEDs, a local on/off switch, and 4-pin Molex Power-In connector
- One DNR-CPU-1000 dual-slot CPU/NIC module with indicating LEDs, two Ethernet connectors (Main and Diagnostic Ports), sync connector, reset pushbutton, SD card slot, USB controller/slave ports (future use), and a DB-9 connector for a serial port
- One DNR-BUFFER Board, for buffering address/control/clock lines (for future use — not currently addressable)
- Up to 12 PowerDNR front pull-out I/O modules (boards) functionally identical to PowerDNA I/O boards but designed for mounting in a DNR rack enclosure
- One DNR-BP-12 Backplane with two temperature sensors
- DNR-IO-FILLER blank filler panels for all unused slots

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- Four 8-volt cooling fans mounted on the rear of the enclosure

NOTE: Note that the rightmost module (Module 11) is 2-slots wide (to accommodate future designs and/or custom modules.

Also note that the DNR-12 enclosure has reversible mounting flanges designed for rack or surface mounting. Rubber feet are supplied for desktop or tabletop mounting.

The enclosure is a rigid mechanical structure with complete EMI shielding. Unused slots are filled with blank brackets and filler panels. The DC/DC power module provides output voltages of 24, 3.3, 2.5, 1.5, and 1.2 VDC for the logic/CPU and 8 VDC to power the four cooling fans.

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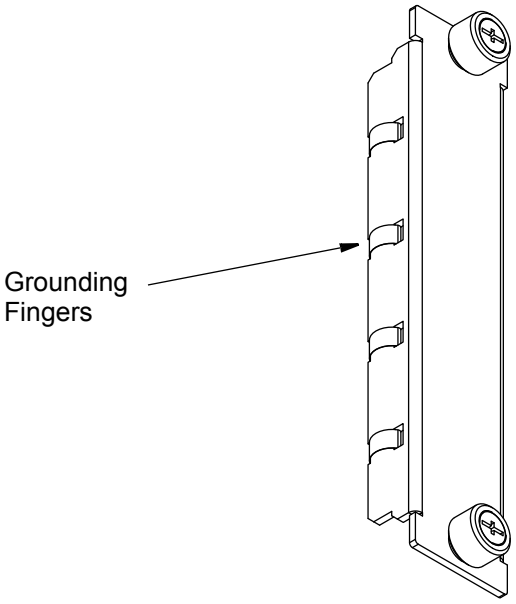


Figure 2-5. Optional DNR-IO-Filler Panel for empty slots

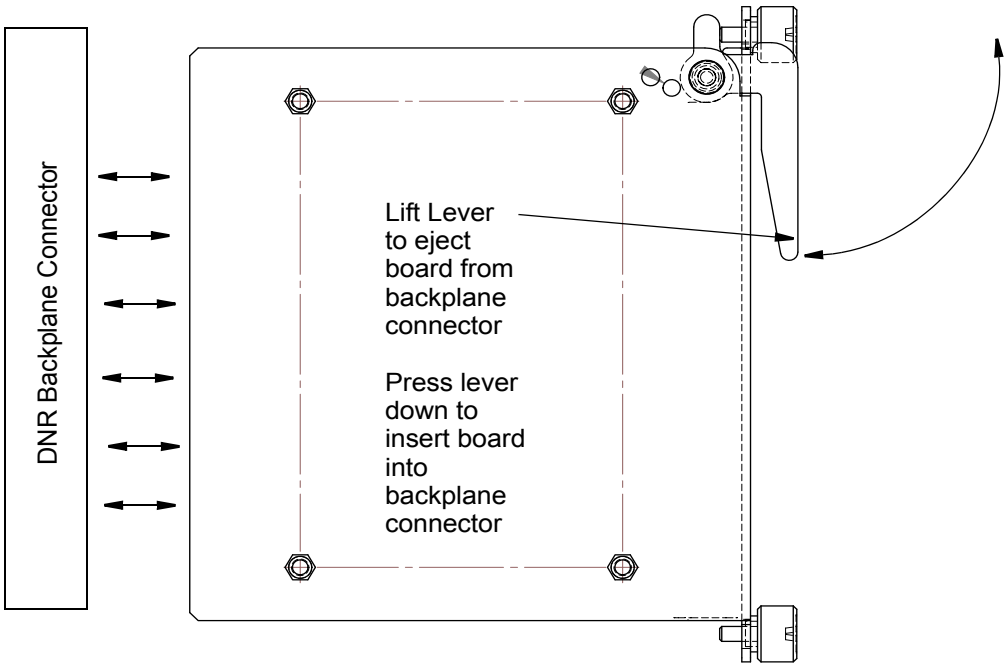


Figure 2-6. DNR Ejection/Insertion Lever Operation

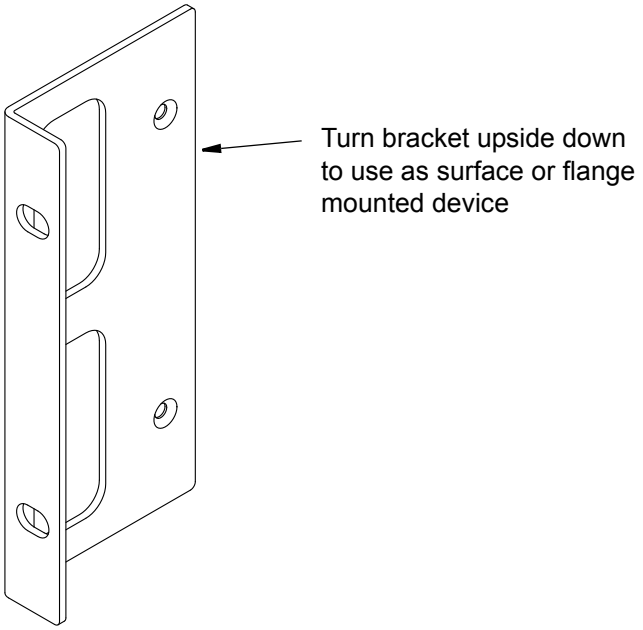


Figure 2-7. DNR-BRACKET Reversible Mounting Bracket

2.4.1 Cooling Air Flow

As shown in **Figure 2-8**, cooling air is drawn into the rear of the enclosure, routed forward over the electronic circuit boards, up to the top of the enclosure, and then out the top rear of the enclosure. The system is designed to maintain positive pressure cooling within the enclosure at all times.

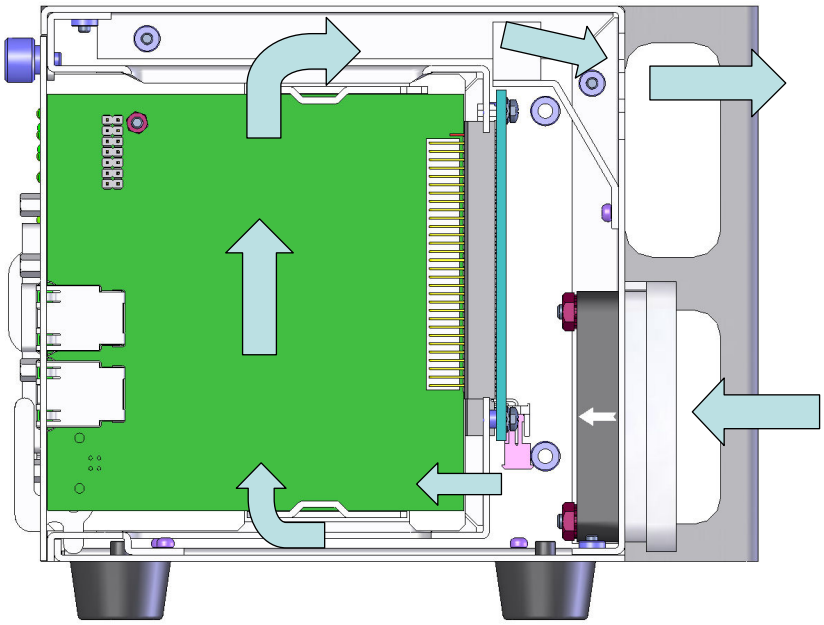
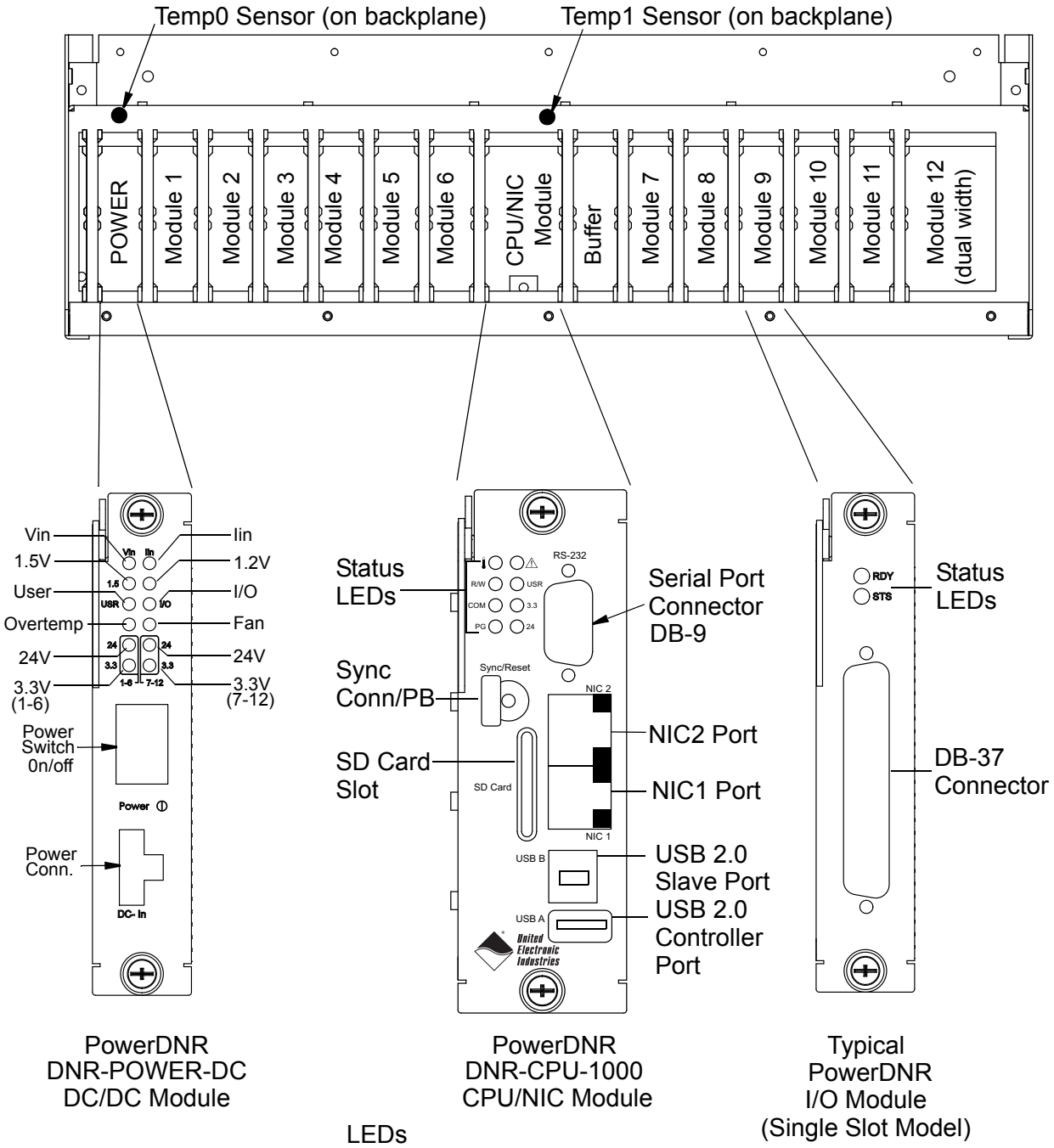


Figure 2-8. DNR-12 Air Flow

2.4.2 DNR Power, CPU/NIC, and I/O Modules

This section describes the basic modules included in every DNR-12-1G system, the CPU/NIC module, the DC/DC power module, buffer module, and I/O modules.



LEDs

ATT Indicates error when red
R/W Flashes when bus is active
COM Flashes when SD Card is read/written
PG Indicates presence of valid power input

Figure 2-9. DNR-12-1G System Front Panel Arrangement

Figure 2-10, **Figure 2-11**, and **Figure 2-12** describe the conditions indicated by the LEDs on the front of each module in the rack.

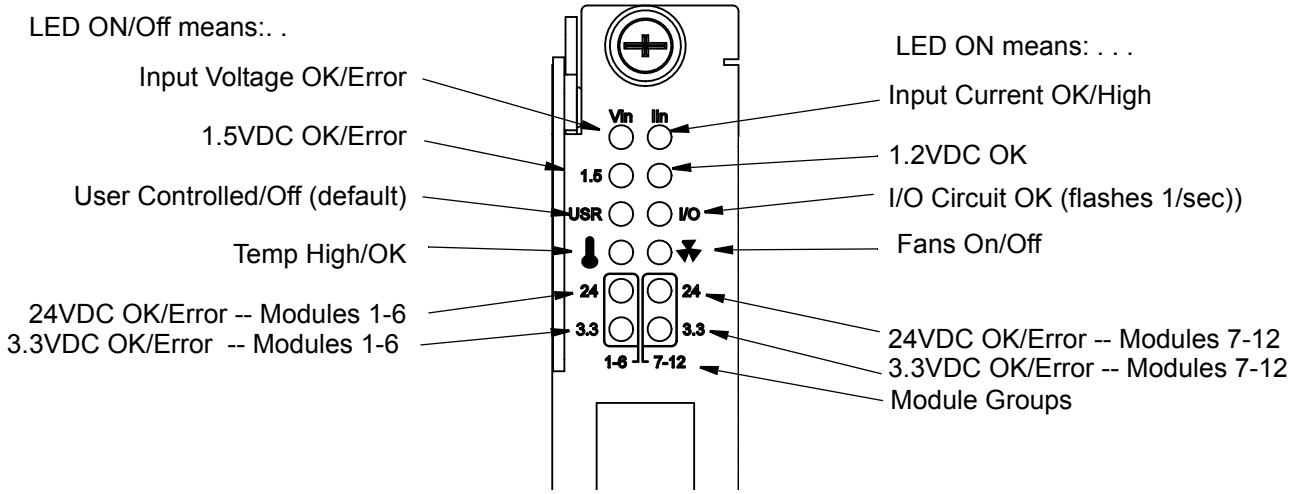


Figure 2-10. DC Power Module LEDs

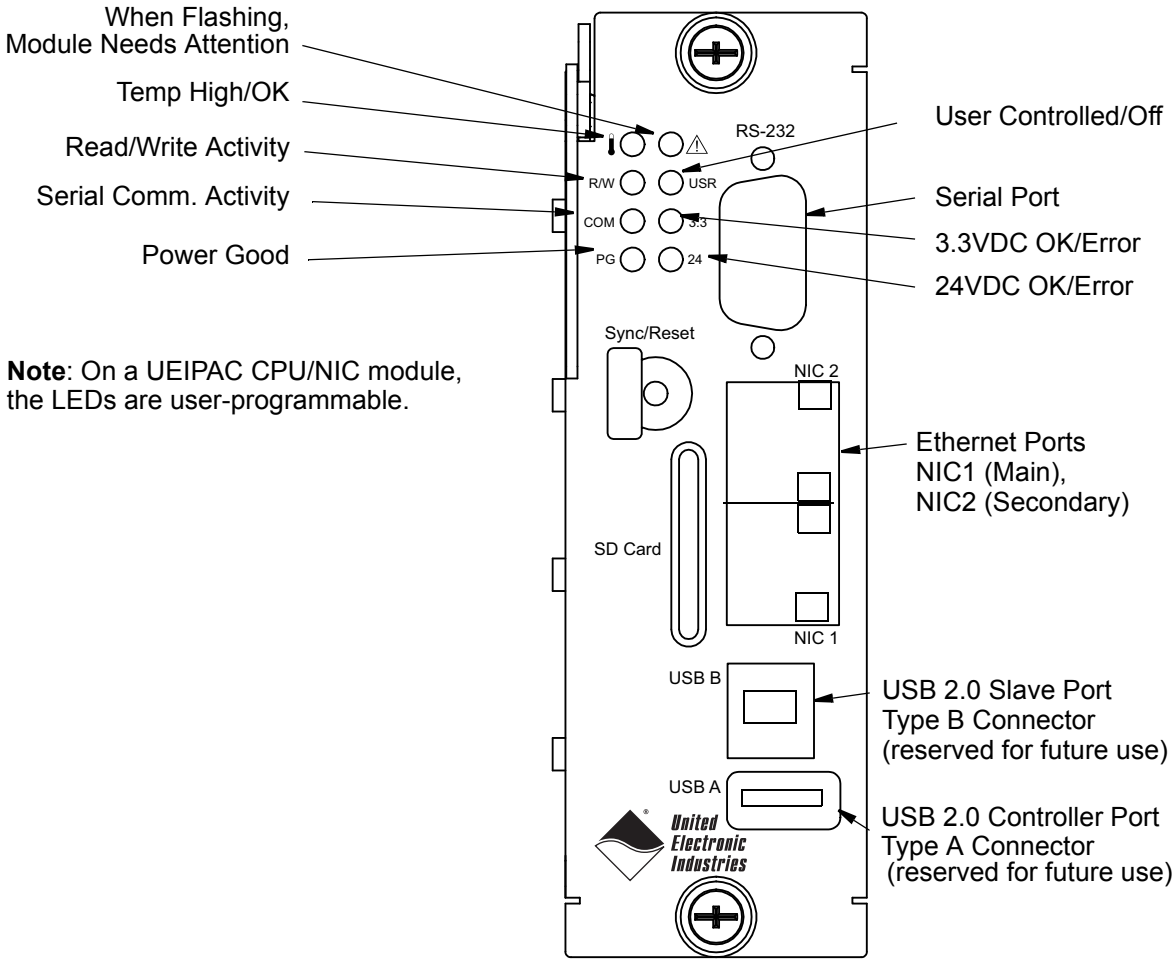


Figure 2-11. DNR-CPU-1000 Module LEDs

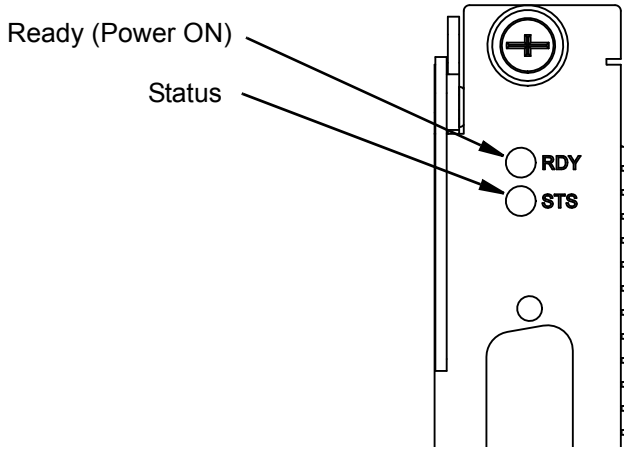


Figure 2-12. Typical I/O Module LEDs

Two sensors mounted on the backplane over the Power Module and over the CPU board monitor internal temperatures continuously, turning fans on if the internal temperature exceeds 45°C, off if it falls below 45°C, and shutting down power if a high limit is exceeded.

All UEI PowerDNA modules are available in both PowerDNA and Power DNR package designs.

A feature of the design is that the address of a module is determined by the position of the module within the enclosure, numbered from left to right. A typical module address is:

0xA00nxxxx

where **A00** is the BASE address
n is the module position number starting from 0 at the left
xxxx is the address of the module

With this addressing method, the address of a given I/O board (module) automatically changes if you move it from one position to another within the enclosure.

The slots or module positions are numbered as follows:

Physical Position (L-R)	Position Number	Module Description
1	0xC	POWER-DC
2	0x0	Module1
3	0x1	Module2
4	0x2	Module3
5	0x3	Module4
6	0x4	Module5
7	0x5	Module6
8	0xD 0xE	POWER-1GB CPU/NIC
9	N/A	BUFFER
10	0x6	Module7
11	0x7	Module8
12	0x8	Module9
13	0x9	Module10
14	0xA	Module11
15	0xB	Module12

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2.5 DNR-POWER-DC Module

The DNR-POWER-DC Module is a dedicated DC/DC source and control module available only for use with a PowerDNR rack enclosure. It is always mounted in the leftmost slot of the DNR chassis and is recognized on the PowerDNR bus with an ID of 0x020 at address 0xA00C0000.

The non-isolated side (NIS) logic complies with full common logic interface (CLI) implementation. The key features of the DNR-POWER Module are:

- Input power — 9-36 VDC 80W maximum, protected by resettable fuses and EMI chokes
- Power supply on/off switch (with guard)
- Output power sources (all with greater than 90% efficiency)

  24V, 1A (24W)
  3.3V, 5A (16.5W, including the 2.5V derived voltage)
  2.5V, 3A (derived from 3.3V source)
  1.5V, 5A, (7.5W, including the 1.2V derived voltage)
  8V, 0.5A (4W for fans)
- DC/DC for 24V, 3.3V, and 1.5V are synchronized from the single spread-spectrum clock source in the CPU/NIC Module for lower EMI noise level
- Fan control (Forced ON) and status ON/OFF
- Monitoring and LED indicators (1% accuracy, 0.25Hz update rate) for:

  – All output voltages
  – Input current for the 9-36VDC for the DNR Enclosure
  – All voltages from the NIC Module (24V, 3.3V, 2.5V)
  – Temperature of the DNR backplane (2 sensors)
- Onboard FPGA logic chip is CYCLONE EP1C3/C6T144
- TI MSP4300 microcontroller used for logic reprogramming
- Input-Output connector is a 128-pin component that provides 9-36VDC for all modules from an external power source

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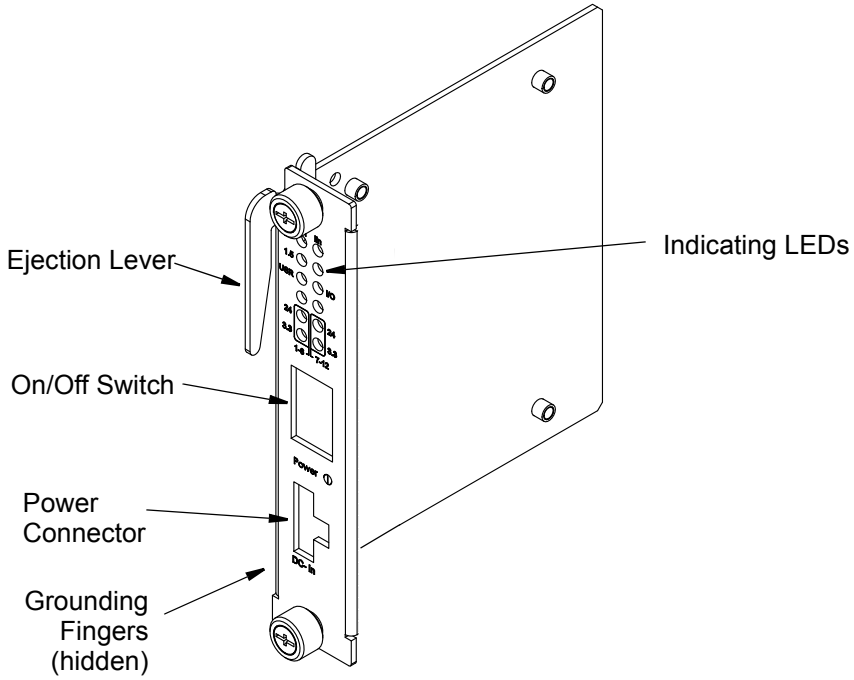

Figure 2-13. DNR-POWER-DC Module

A functional block diagram of the DNR-POWER-DC Module is shown in **Figure 2-14** below.

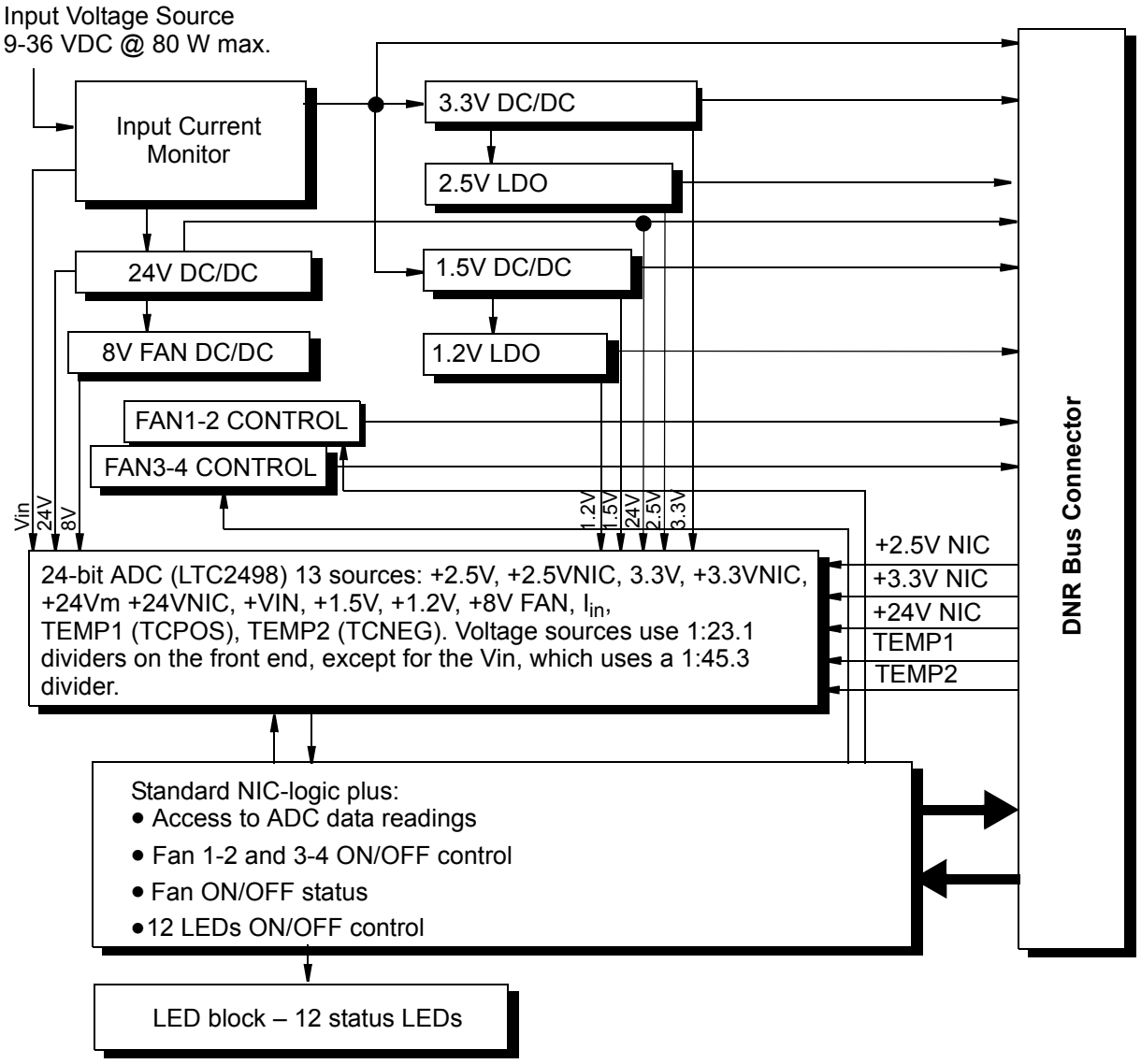

Figure 2-14. Functional Block Diagram of DNR-POWER-DC Module

As shown in **Figure 2-14**, the DNR-POWER-DC Module operates as follows:

A 9-36VDC voltage input (Vin) from an external source is connected to the board through a replaceable slow-blow fuse. The board monitors the input current and passes Vin to the DNR bus as Vout. Vout also is connected to DC/DC converters that produce 24 VDC, 3.3VDC and 1.5VDC output voltages, which are also placed on the DNR bus. Both 3.3 and 1.5VDC voltages are connected to low dropout regulators that, in turn, generate the 2.5VDC and 1.2VDC output voltages on the bus. The 24VDC source is fed to a low dropout regulator that produces 8VDC to drive the cooling fans (through fan controller chips).

The input current and all output voltages, including the +2.5, +3.3, and +24VDC from the NIC module, plus signals from the two temperature sensors mounted within the enclosure, are input to a 24-bit delta-sigma A/D converter. Except for Vin, the voltage sources use 1:23.1 dividers on the front end. Vin uses a 1:45.3 divider.

Figure 2-15 shows the interaction of modules within a DNR-12-ENCL Enclosure when the DNR-BUFFER module is used.

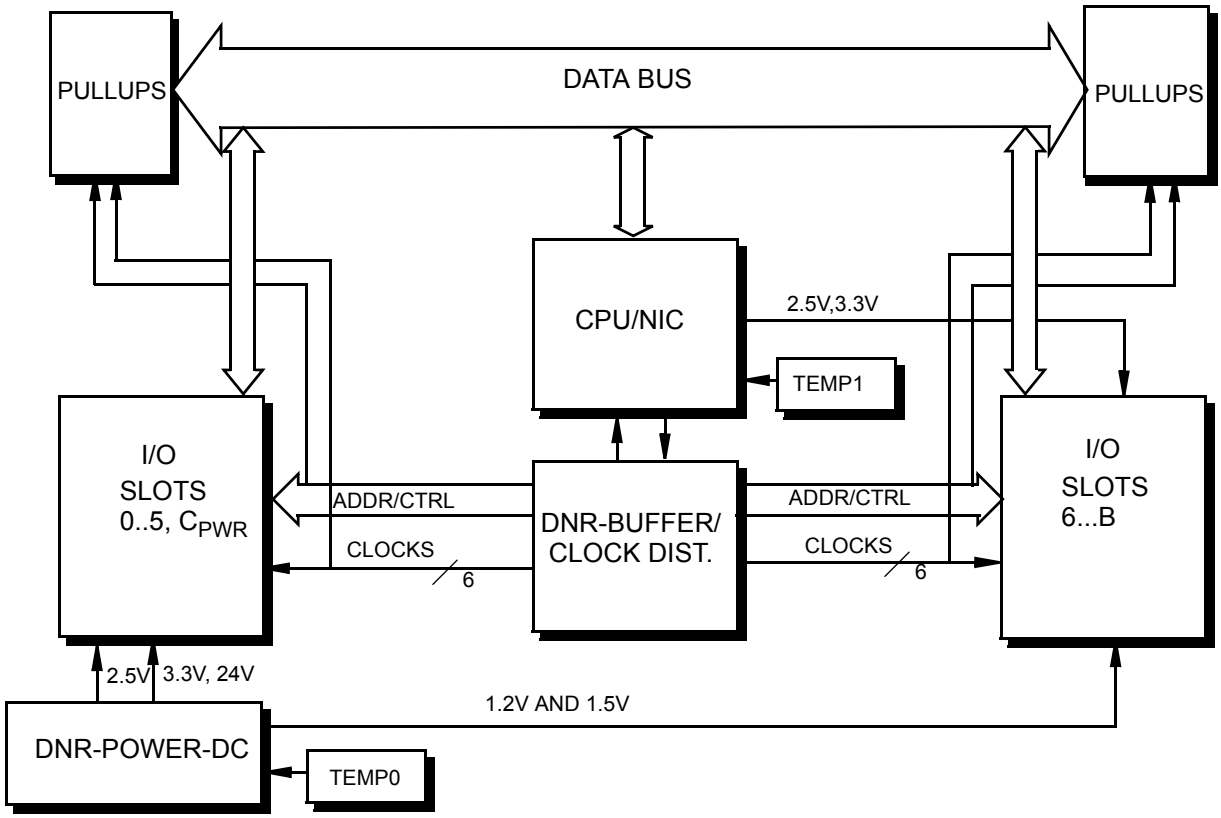

Figure 2-15. Functional Block Diagram of DNR-12-ENCL

As shown above, the I/O slots are divided into two groups: 0 to 5 and 6 to 0xB. 0xC for the DC Power Module is included with the 0 to 5 group. The DNR-BUFFER board is located at the center of the enclosure, which is also at the center point of the ADDR/CTRL bus. The DNR-CPU-1000 module is also located at the center of the enclosure and the center of the data bus to minimize bus delays. The CPU addresses I/O modules and transmits clock ticks through the Buffer Board, which controls the Addr/Ctrl and clock lines to the modules.

Temperature sensors monitor temperatures within the enclosure above the DNR-POWER-DC module and the DNR-CPU module.

2.6 DNR-CPU/NIC Module

The DNR-CPU-1000 Module contains a PowerPC 8347 CPU and associated Network Interface Control (NIC) logic that controls all Ethernet communication functions. The DNR-CPU-1000 has a dual 1-GB Ethernet module.

2.7 DNR-Buffer Module

The DNR-BUFFER Module provides buffering between the CPU and I/O module address/control/clock lines, which functions as described in **Figure 2-15**. Although the module may not always be required, it is included to provide an extra margin of safety against loss of data.

2.8 DNR-IO-Modules

All standard PowerDNA I/O modules are also available as PowerDNR modules. A typical PowerDNR module has functions that are functionally identical to its corresponding PowerDNA version. The only difference between them is the physical mounting arrangement. PowerDNR modules are designed for insertion into the DNR-12-ENCL enclosure; PowerDNA modules can be inserted only into a PowerDNA Cube.

Therefore, for detailed electrical specifications and user instructions for a specific DNR I/O board, refer to the datasheets and User Manuals for the equivalent PowerDNA I/O module. These documents are available for examination and download from the UEI website at www.ueidaq.com.

2.9 DC Power Thresholds

Table 2-1 lists the DC power threshold specifications for DNR-12-1G 12-slot RACKtangle systems.

Table 2-1 DC Power Thresholds for DNR-X-1G RACKtangle and HalfRACK systems

	Backplane Power Rail Voltages	Turn-on Voltage, V[1]	Reset Voltage, V	Turn-off Voltage, V[2]	Notes
Logic power supply	+3.3V, +2.5V, +1.5V, +1.2V	7.5	7.2 (When Vin is below 7.2V, a voltage reset puts all layers into reset mode.)	7.0	Supplies power to all CPUs and FPGAs. DNR can communicate with Ethernet when CPU is functional
Analog power supply	+24V	8.5	-	7.8	Analog power supply is used as a regulated source for on-layer DC/DCs on most layers
Fan power supply	+12V	8.5	-	8.4	
On-layer DC/DCs that use input power	+VIn	7.8-8.8	-	7.5-8.5	Varies with layer type.

1. Turn-on, V: The value of Vin at which the corresponding DC/DCs are turned on.
2. Turn-off, V: The value of Vin at which the corresponding DC/DCs are turned off.

NOTE: A DNR-12-1GB CPU/NIC core module consumes only 70mW when Vin is below 7V.

Chapter 3 The DNR-6-1G *HalfRACK* System

3.1 System Overview

The UEI PowerDNR DNR-6-1G *HalfRACK™* product is identical to the DNR-12-1G system except for the size of the enclosure and the number and order of I/O modules it can accept. All standard PowerDNA I/O boards are available in PowerDNR versions for use in DNR-6-1G systems.

Figure 3-1. Typical DNR-6-1G HalfRACK™ System

As illustrated in **Figure 3-3** and **Figure 3-5** on page 27, a standard DNR-6-1G PowerDNR *HalfRACK* system consists of the following modules:

- One or more DNR-6-ENCL rack mounted enclosures
- DNR-POWER-DC Power Module (one for each enclosure)
- DNR-CPU-1000 Module (Freescale MPC8347 CPU and 1-GB Ethernet 1000 Base-T Network Interface Module — one for each enclosure)
- DNR-IO-FILLER panels (one for each unused I/O slot)
  Note: These slot covers are optional and not included in the price of the rack.
- DNR-PSU-24-100 100-Watt, 120/230 VAC to +24VDC External Power Supply (one for each enclosure) with cable and Molex connector for plug-in to the DNR-POWER-DC Module front panel.

To configure a complete data acquisition system, insert up to 6 DNR I/O modules into each PowerDNR rack enclosure, which may be specified in any combination of the following types:

- DNR-AI-201, -202, 205, 207, -208, -211, -225
- DNR-AO-308, -308-350, -308-353, -308-420, -332,
- DNR-DIO-401, -402, -403, 404, -405, 406, -416, -432, -433, -448
- DNR-CT-601, DNR-QUAD-604
- DNR-SL-501, DNR-CAN-503
- DNR-429-566, DNR-429-512

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- DNR-GPS
- Any future additions to the PowerDNR I/O module product line

Note: Refer to www.ueidaq.com for a description of each I/O module.

All standard PowerDNA accessories are also available for use in a DNR-6-1G *HalfRACK* system.

NOTE: UEIPAC, UEISIM, and UEIModbus deployments are now available for use with DNR-6 HalfRACK systems, with the following model names:

- UEIPAC — UEIPAC 600R
- UEISIM — UEISIM 600R
- UEIModbus — UEIModbus 600R

3.2 Specifications

The technical specifications of the DNR-6-1G *HalfRACK* system are listed below.

Technical Specifications:

Standard Interfaces	
To Host Computer	Two independent 1000Base-T Gigabit Ethernet ports (100/10Base-T compatible)
Distance from host	100 meters, max
Other Interfaces	One USB 2.0 controller port, One USB 2.0 slave port.
Config/General	RS-232, 9-pin "D"
Sync	Custom cable to sync multiple racks
I/O Slots Available	
DNR-6-1G	6 slots
Data transfer and communications rates	
Ethernet data transfer rate	20 megabytes per second
Analog data transfer rate	up to 6 megasample per sec (16-bit samples)
DMAP I/O mode	update 1000 I/O channels (analog and/or digital) in less than 1 millisecond, guaranteed
Processor	
CPU	Freescale 8347, 400 MHz, 32-bit
Memory	128 MB (not including on-board Flash)
Status LEDs	Power supplies within spec, One second system heart-beat, Attention, Read/Write, Power, Communications Active
Environmental	
Temp (operating)	Tested to -40 °C to 70 °C
Temp (storage)	-40 °C to 85 °C
Humidity	0 to 95%, non-condensing
Vibration	
(IEC 60068-2-64)	10–500 Hz, 3 g (rms), Broad-band random
(IEC 60068-2-6)	10–500 Hz, 3 g, Sinusoidal
Shock	
(IEC 60068-2-27)	50 g, 3 ms half sine, 18 shocks at 6 orientations; 50 g, 11 ms half sine, 18 shocks at 6 orientations
MTBF	130,000 hours
Physical Dimensions	
DNR-6 series	5.25" x 6.2" x 17.5" (3U in a 19" rack)
Power Requirements	
Voltage	9 - 36 VDC (AC adaptor included)
Fuse	Internal 10 A
Power Dissipation	13 W at 24 VDC (not including I/O boards)
Power Monitoring	
I/O board power	All internal power supplies monitored to ±1% accuracy. All PS voltages may be read by host. LED annunciators indicate out of range
Input current	Monitored by host, LED indicates overcurrent
Input voltage	Monitored by host, LED indicates out of range

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3.3 Key Features

The following table is a list of key features of a DNR-6-1G *HalfRACK* system.

DNR Series Advantages:

Easy to Configure and Deploy

- Over 30 different I/O boards available
- Over 5 quadrillion possible configurations
- Gigabit Ethernet based (100/10Base-T compatible)
- Bracket kit for mounting to wall or in 19" racks
- Industrial quality rubber feet for solid table-top mounting
- Passive backplane ensures extremely low MTTR
- Standard "Off-the-shelf" products and delivery

True Real-time Performance

- 1 msec updates guaranteed with 1000 I/O
- Up to 6 million samples per second
- Use QNX, RTX, RT Linux, RTAI Linux, LabVIEW RT

Flexible Connectivity

- 1000Base-T with Cat-5 cable
- Supports WIFI / GSM / Cell networks
- Built-in USB 2.0 slave and controller ports

Compact Size:

- 5.25" x 6.2" x 17.5"
- 300 analog inputs per rack
- 384 analog outputs per rack
- 576 digital I/O bits per rack
- 96 counter/quadrature channels per rack
- 144 ARINC-429 channels per rack
- 48 RS-232/422/485 ports per rack

Low Power:

- Less than 13 watts per typical rack (not including I/O)
- AC, 9-36 VDC or battery powered.

Stand alone and Data Logger Modes

- Upgradable to UEILogger 600R
- Upgradable to UEIPAC 600R
- Upgradable to UEIModbus 600R

Rugged and Industrial:

- Solid Aluminum construction
- 130,000 hour MTBF
- Operation tested from -40°C to +70°C
- Vibration tested to 3 g, (operating)
- Shock tested to 50 g (operating)
- All I/O isolated from rack and host PC.

Outstanding Software Support

- Windows, Linux, RT Linux, Windows RT, RTX VXworks and QNX operating systems
- VB, VB .NET, C, C#, C++, J#
- MATLAB, LabVIEW, DASYLab, OPC, ActiveX support

Figure 3-2. DNR-6-1G HalfRACK Product Features

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3.4 DNR-6-1G *HalfRACK* System Enclosure

Each DNR-6-1G enclosure contains a DNR-POWER-DC Power Module with status indicating LEDs and a local ON/OFF switch — and each I/O module is provided with a mechanical lever (see **Figure 2-6** on page 9) for quick ejection and insertion of the board. In addition, each DNR-6-1G system enclosure also contains its own GigE CPU and two Network Interface Control (NIC) modules, one for controlling up to 6 I/O modules mounted in the enclosure, and another for diagnostic functions. The module-specific I/O boards are functionally identical to the corresponding modules for the PowerDNA Cube.The only differences between the two types relate to the mounting arrangements.

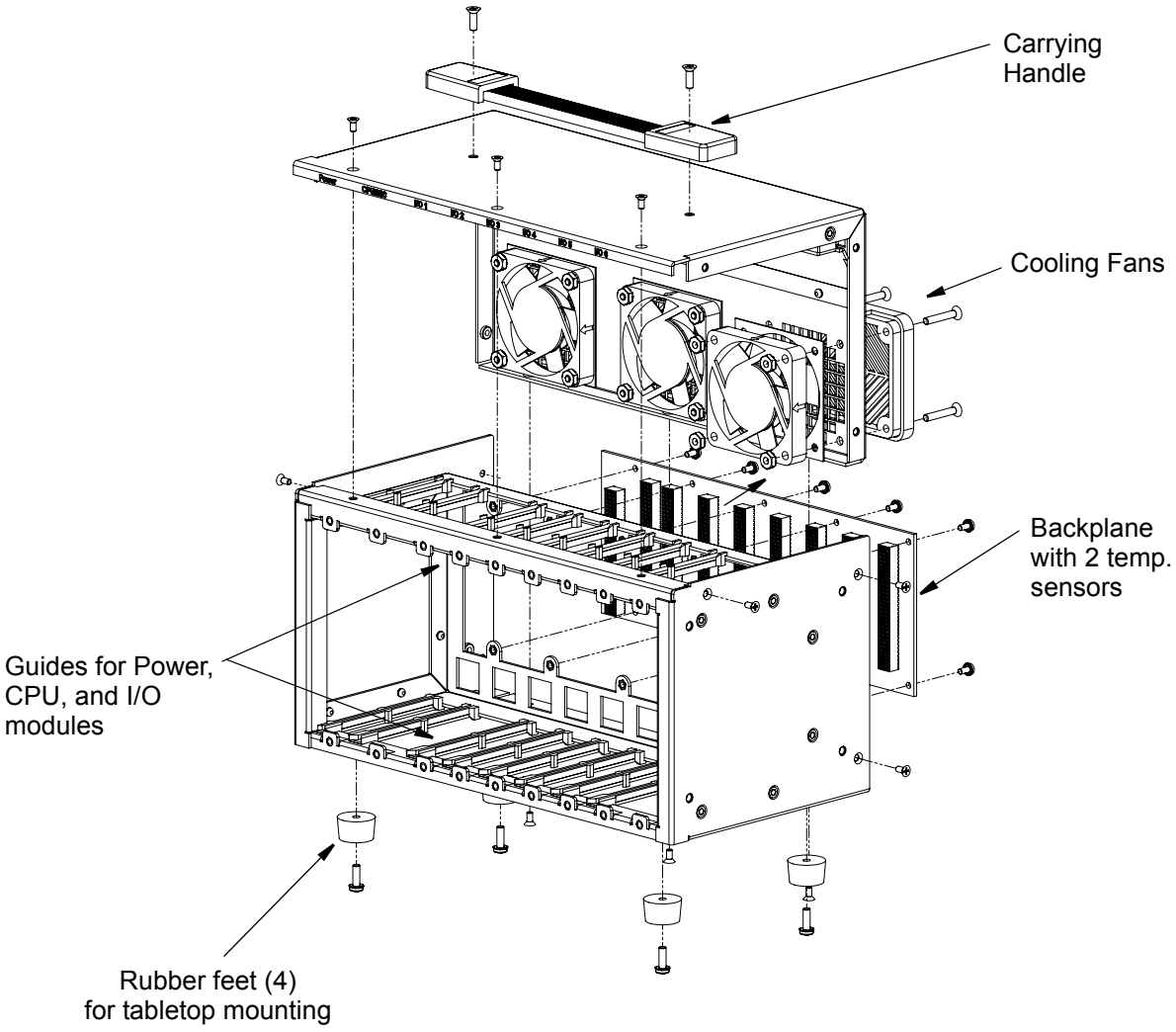

Carrying Handle
Cooling Fans
Backplane with 2 temp. sensors
Guides for Power, CPU, and I/O modules
Rubber feet (4) for tabletop mounting

Figure 3-3. Typical HalfRACK DNR-6-ENCL Enclosure (Exploded View)

As shown in **Figure 3-3** and **Figure 3-5**, the DNR-6 enclosure is designed to house the following items:

- One isolated DNR-POWER-DC DC/DC Power Module/Power Monitor with status indicating LEDs, a local on/off switch, and 4-pin Molex Power-In connector

- One DNR-CPU-1000 dual-slot CPU/NIC module with indicating LEDs, two Ethernet connectors (Main and Diagnostic Ports), sync connector, reset pushbutton, SD card slot, USB controller/slave ports (future use), and a DB-9 connector for a serial port
- Up to 6 PowerDNR front pull-out I/O modules (boards) functionally identical to PowerDNA I/O boards but designed for mounting in a DNR rack enclosure
- One DNR-BP-6 Backplane with two temperature sensors
- DNR-IO-FILLER blank filler panels for all unused slots
- Three 8-volt cooling fans mounted on the rear of the enclosure

NOTE: Note that the rightmost module (Module 6) is 2-slots wide (to accommodate future designs and/or custom modules. Rubber feet are supplied for desktop or tabletop mounting. If flange mounting is desired, contact UEI for more information.

The enclosure is a rigid mechanical structure with complete EMI shielding. A convenient carrying handle is also provided for portability. Unused slots should be filled with blank filler panels. The DC/DC power module provides output voltages of 24, 3.3, 2.5, 1.5, and 1.2 VDC for the logic/CPU and 8 VDC to power the three cooling fans.

3.4.1 Cooling Air Flow

As shown in **Figure 3-4**, cooling is drawn into the rear of the enclosure, routed forward over the electronic circuit boards, up to the top of the enclosure, and then out the top rear of the enclosure. The system is designed to maintain positive pressure cooling within the enclosure at all times.

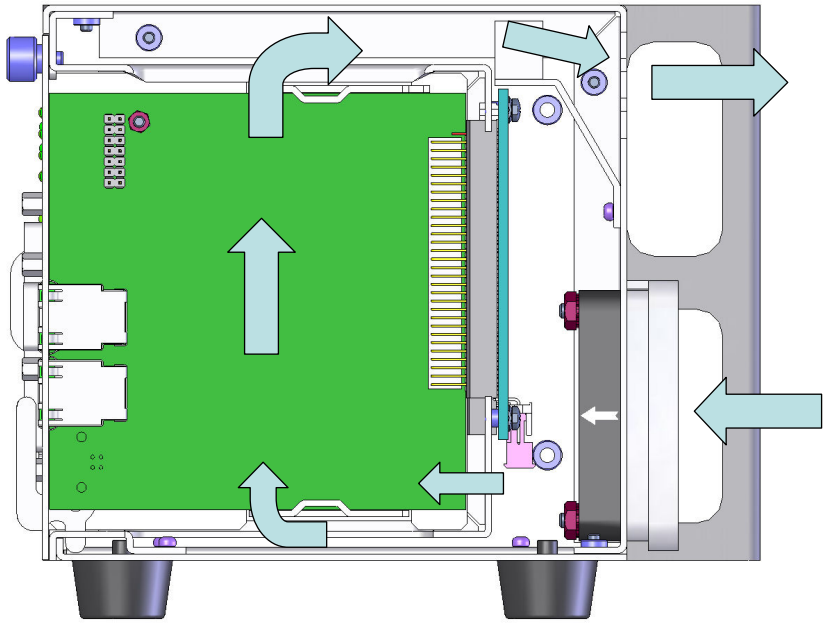
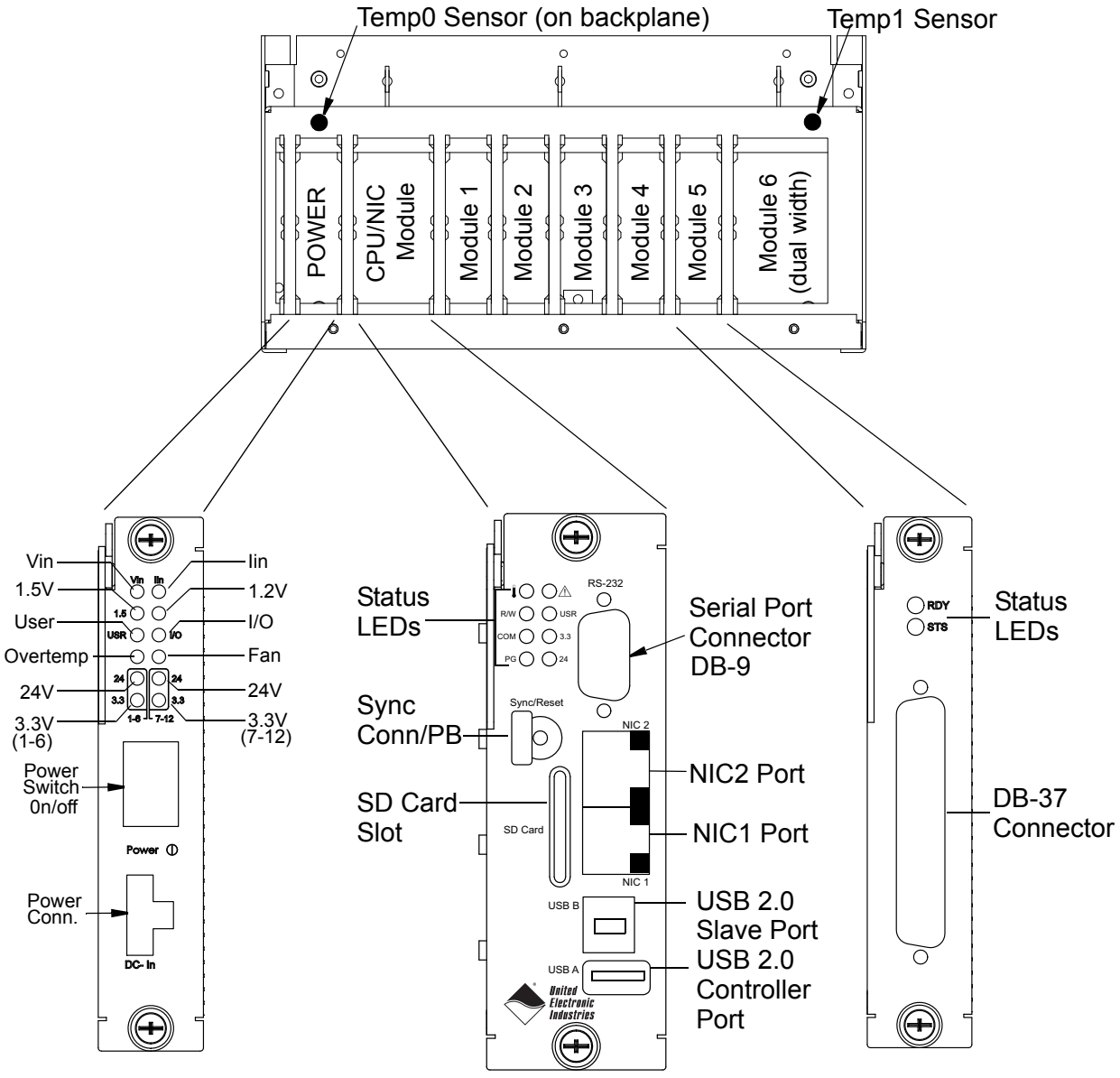


Figure 3-4. DNR-6 Air Flow

3.4.2 DNR-6 Power, CPU/NIC, and I/O Modules

This section describes basic modules included in every DNR-6-1G system, the CPU/NIC module, the DC/DC power module, and I/O modules. Note that modules used in both DNR-6 and DNR-12 systems are identical. The DNR-6 enclosure, however, only accepts six I/O modules.



LEDs

ATT Indicates error when red
R/W Flashes when bus is active
COM Flashes when SD Card is read/written
PG Indicates presence of valid power input

Figure 3-5. DNR-6-1G System Front Panel Arrangement

Figure 3-6, **Figure 3-7**, and **Figure 3-8** describe the conditions indicated by the LEDs on the front of each module in the rack.

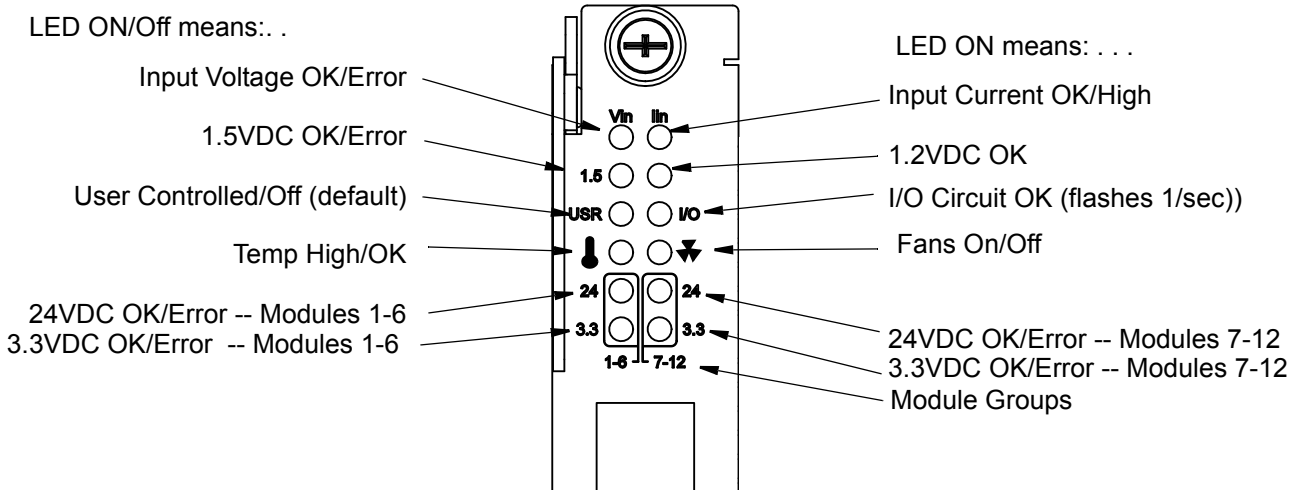


Figure 3-6. DC Power Module LEDs

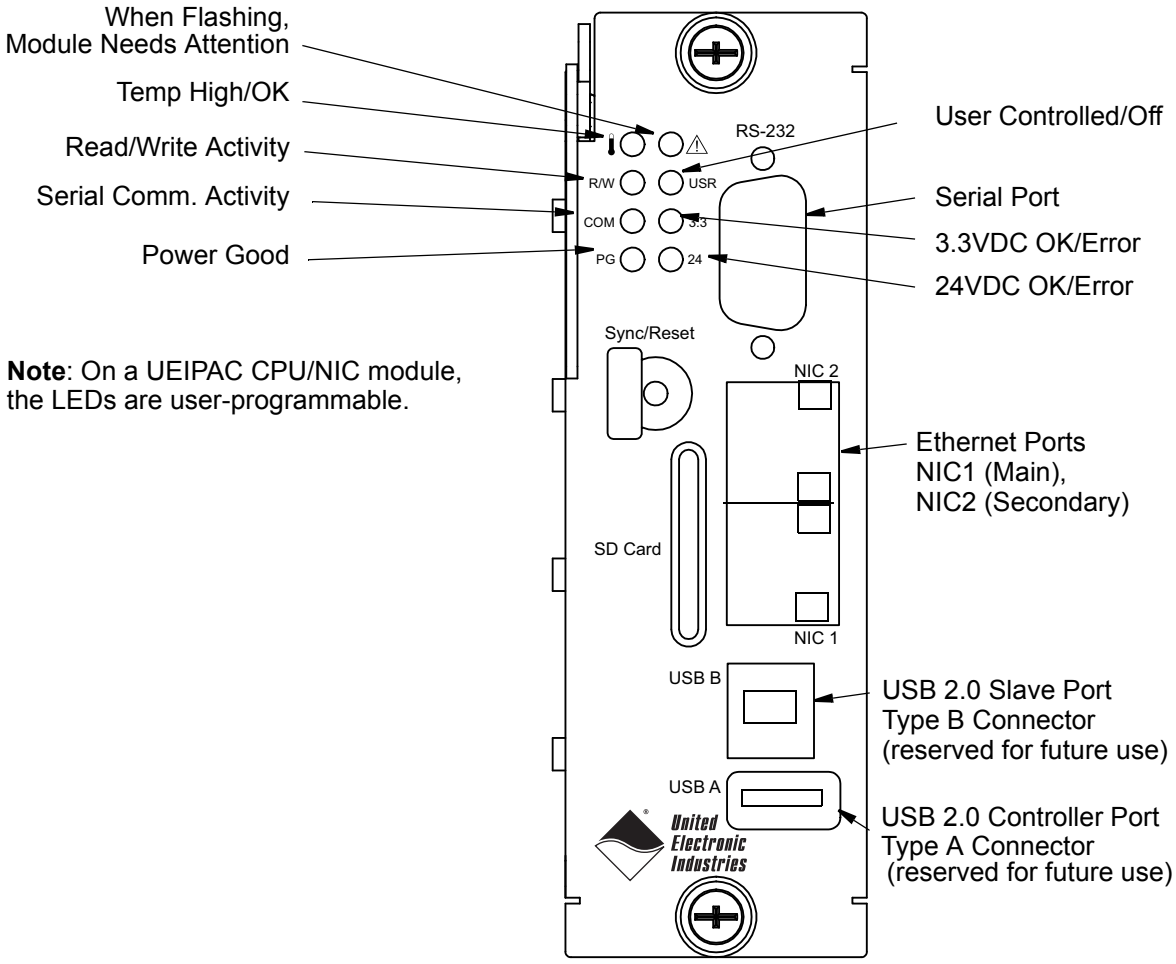


Figure 3-7. DNR-CPU-1000 Module LEDs

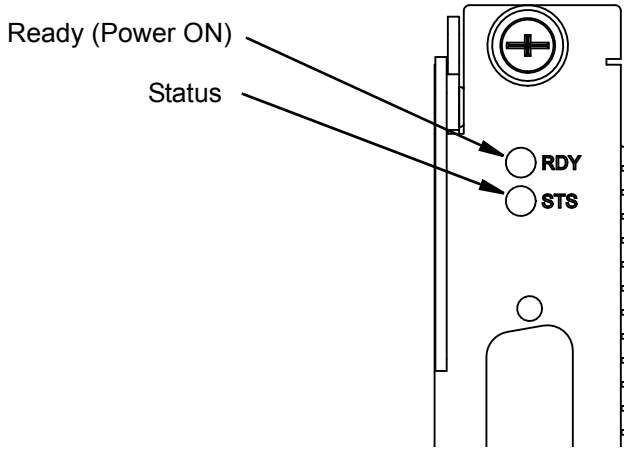


Figure 3-8. Typical I/O Module LEDs

Two sensors mounted on the backplane monitor internal temperatures continuously, turning fans on if the internal temperature exceeds 45°C, off if it falls below 45°C, and shutting down power if a high limit is exceeded.

All UEI PowerDNA modules are available in both PowerDNA and Power DNR package designs.

A feature of the design is that the address of a module is determined by the position of the module within the enclosure, numbered from left to right. A typical module address is:

0xA00nxxxx

where **A00** is the BASE address
n is the module position number starting from 0 at the left
xxxx is the address of the module

With this addressing method, the address of a given I/O board (module) automatically changes if you move it from one position to another within the enclosure.

The slots or module positions for the DNR-6-1G are numbered as follows:

Physical Position (L-R)	Position Number	Module Description
1	0xC	POWER-DC
2	0xD 0xE	POWER-1GB CPU/NIC
3	0x0	Module1
4	0x1	Module2
5	0x2	Module3
6	0x3	Module4
7	0x4	Module5
8	0x5	Module6

3.5 DNR-POWER-DC Module

Refer to See “DNR-POWER-DC Module” on page 16. in Chapter 2 for a detailed description of the DNR-POWER-DC Module.

3.6 DNR-CPU/NIC Module

The DNR-CPU-1000 Module contains a PowerPC 8347 CPU and associated Network Interface Control (NIC) logic that controls all Ethernet communication functions. The DNR-CPU-1000 has a dual 1-GB Ethernet module. This unit is used in both the DNR-6 and the DNR-12 systems.

3.7 DNR-IO-Modules

All standard PowerDNA I/O modules are also available as PowerDNR modules. A typical PowerDNR module has functions that are functionally identical to its corresponding PowerDNA version. The only difference between them is the physical mounting arrangement. PowerDNR modules are designed for insertion into the DNR-6-ENCL or DNR-12-ENCL enclosure; PowerDNA modules can be inserted only into a PowerDNA Cube.

Therefore, for detailed electrical specifications and user instructions for a specific DNR I/O board, refer to the datasheets and User Manuals for the equivalent PowerDNA I/O module. These documents are available for examination and download from the UEI website at www.ueidaq.com.

3.8 DC Power Thresholds

Table 3-1 lists the DC power threshold specifications for DNR-X-1G HalfRACK systems.

Table 3-1 DC Power Thresholds for DNR-6-1G HalfRACK Systems

	Backplane Power Rail Voltages	Turn-on Voltage, V[1]	Reset Voltage, V	Turn-off Voltage, V[2]	Notes
Logic power supply	+3.3V, +2.5V, +1.5V, +1.2V	7.5	7.2 (When Vin is below 7.2V, a voltage reset puts all layers into reset mode.)	7.0	Supplies power to all CPUs and FPGAs. DNR can communicate with Ethernet when CPU is functional
Analog power supply	+24V	8.5	-	7.8	Analog power supply is used as a regulated source for on-layer DC/DCs on most layers
Fan power supply	+12V	8.5	-	8.4	
On-layer DC/DCs that use input power	+VIn	7.8-8.8	-	7.5-8.5	Varies with layer type.

1. Turn-on, V: The value of Vin at which the corresponding DC/DCs are turned on.
2. Turn-off, V: The value of Vin at which the corresponding DC/DCs are turned off.

NOTE: A DNR-6-1GB CPU/NIC core module consumes only 70mW when Vin is below 7V.

Chapter 4 Installation and Configuration

Installation consists of:

- DNR-6-1G or DNR-12-1G hardware setup
- PowerDNA/PowerDNR software package installation
- Configuration

NOTE: Throughout this chapter, several figures include graphic representations of DNR-12 systems. Each such figure could also be shown with a DNR-6 system instead of a DNR-12 unit.

4.1 Initial Installation Guide

This section describes the procedure recommended for performing an initial hardware and software setup when you first receive a DNR-X-1G system.

4.1.1 Inspect Package

Inspect the contents of the shipping package. With a standard DNR-X-1G system, you should find:

- A DNR-12-ENCL or DNR-6-ENCL enclosure, preinstalled with a DNR-CPU-1000 module, DNR-POWER-DC module, blank filler panels (if specified), plus your selection of I/O Boards. A DNR-12 system also includes a DNR-BUFFER module (not required with a DNR-6).
- A DNA-PSU-24-100 100-watt[1] universal powerline brick that plugs into an AC outlet and provides 24V dc output. The supply comes with a power cord for the mains and an adapter cable ending in a Molex connector for plugging into the DNR-POWER-DC Module.
- DB-9 serial cable for initial hardware configuration and firmware downloading.
- CD-ROM with support software

NOTE: Depending on your application, you may also need to provide the following items not normally included with your order (see Figures 4-3 to 4-6 on pages 38 to 42):

- CAT5e cables between host and DNR system NIC1 primary port, and/or between host and an Ethernet switch, and/or between switch and DNR primary port
- CAT5e cables between host and DNR system secondary (diagnostic) NIC2 port, between host and an Ethernet switch, and/or between switch and DNR secondary (diagnostic) port

4.1.2 Install Software

This section describes how to load the PowerDNA software suite onto a Windows- or Linux-based computer and run some initial tests.

The latest PowerDNA or DNR-X-1G support software is online at www.ueidaq.com/download; a known working copy is also on the PowerDNA Software Suite CD.

1. A larger power supply is required for some configurations. Refer to UEI.

A. Software Install: Windows 9x/2000/XP

The PowerDNA CD provides one installer that combines the UEI low-level driver and UEIDAQ Framework.

The installer automatically searches for third-party IDE and testing suites, and adds them as tools to the suites found. Be sure to install third-party applications (such as LabVIEW, MATLAB, or MsVS2003) ***before*** installing the PowerDNA Software Suite.

To install the PowerDNA Software Suite, do the following:

STEP 1: Log in as Administrator.

STEP 2: Run Setup

a. Insert the PowerDNA Software Suite CD into your CD-ROM drive. Windows should automatically start the PowerDNA Setup program. An installer with the UEI logo and then PowerDNA Welcome screen should appear. If none appears, run setup.exe from the CD drive:

Start >> Run >> d:\setup.exe >> OK.

If you downloaded the most recent executable from www.ueidaq.com, double-click on the filename to run the executable.

b. Choose the PowerDNA Software Suite option.

c. Unless you are an expert user and have specific requirements, select *Typical Installation* and accept the default configuration. The Software Suite installer requires and automatically installs Sun's Java VM (JRE) for you, in addition to the full complement of tools. As an alternative, use the *Custom* option to display and ensure that all of the necessary packages are installed.

-- Companion Documentation:
Quick Start Guide, Configuration and Core Module, I/O Board Manuals, Low-Level Programming Guide

– SDK: includes/lib for C/Java, examples, and Sun's JRE; (The SDK is not the UeiDaq Framework).

– PowerDNA Apps: PowerDNA Explorer, MTTTY

– PowerDNA Components (incl. DLL files)

– PowerDNA Firmware

d. Click **Next** to continue through the dialogs.

e. Click **Finish** to complete the installation; restart the computer.

This Software Suite installed the bare-minimum tools needed in later steps: MTTTY, PowerDNA Explorer, and the low-level driver.

UEIDAQ Framework provides the structure for developing applications under C/C++, C#, VB.NET, ActiveX (VB6, Delphi), MATLAB, LabVIEW, DASYLab, LabWindows/CVI, OPC, and other programming languages.

NOTE: Because the installation process modifies your Windows registry, you should always install or uninstall the software using the appropriate utilities. Never remove PowerDNA software from your PC directly by deleting individual files; always use the Windows Control Panel Add/Remove Programs utility.

B. Software Install: Linux

Linux: The PowerDNA_*.tgz file in the CD\Linux folder contains the software package for Linux. To extract the file to a local directory:

```
tar -xjvf /path/to/powerdna*.tgz
```

Follow the instructions in the readme.txt file contained therein.

4.2 Initial Boot-up

Perform an initial boot in preparation for configuring the network, using the following procedure:

STEP 1: Familiarize yourself with your DNR system front-panel layout. Note that all connections are made on the front of the unit; no rear access is required in a rack-mounted configuration.

STEP 2: Attach the serial cable to the host PC and to the RS-232 port on the front panel of the DNR-CPU-1000 Module.

a. Run a terminal-emulation program (MTTTY) on the PC. Any terminal-emulation program, except HyperTerminal, may be used (MTTTY, Minicom, TeraTerm, etc.).

b. Verify that COM parameters are set at: 57600 baud, 8 bits, no parity, 1 stop bit.

c. Click **Connect** in MTTTY, or use the commands on one of the other terminal-emulation programs to establish communication with the DNR-X-1G system.

STEP 3: Connect power to the system (9-36V DC) by plugging the Molex-type power connector from the power supply into the mating connector on the DNR-POWER-DC module. The power source may be the bundled DNA-PSU-24-100 100 watt powerbrick or a user-supplied source. Note that the DNA-PSU-24-100 plugs into a 100 - 240V, 47- 63 Hz outlet and outputs up to 4.17A at 24 VDC.

STEP 4: Turn on the ON/OFF power switch on the DNR-POWER-DC Power Module front panel.

STEP 5: As soon as the system powers up, it runs through self-diagnostic mode and generates output on the terminal program. A typical readout might be as shown in **Figure 4-1**:

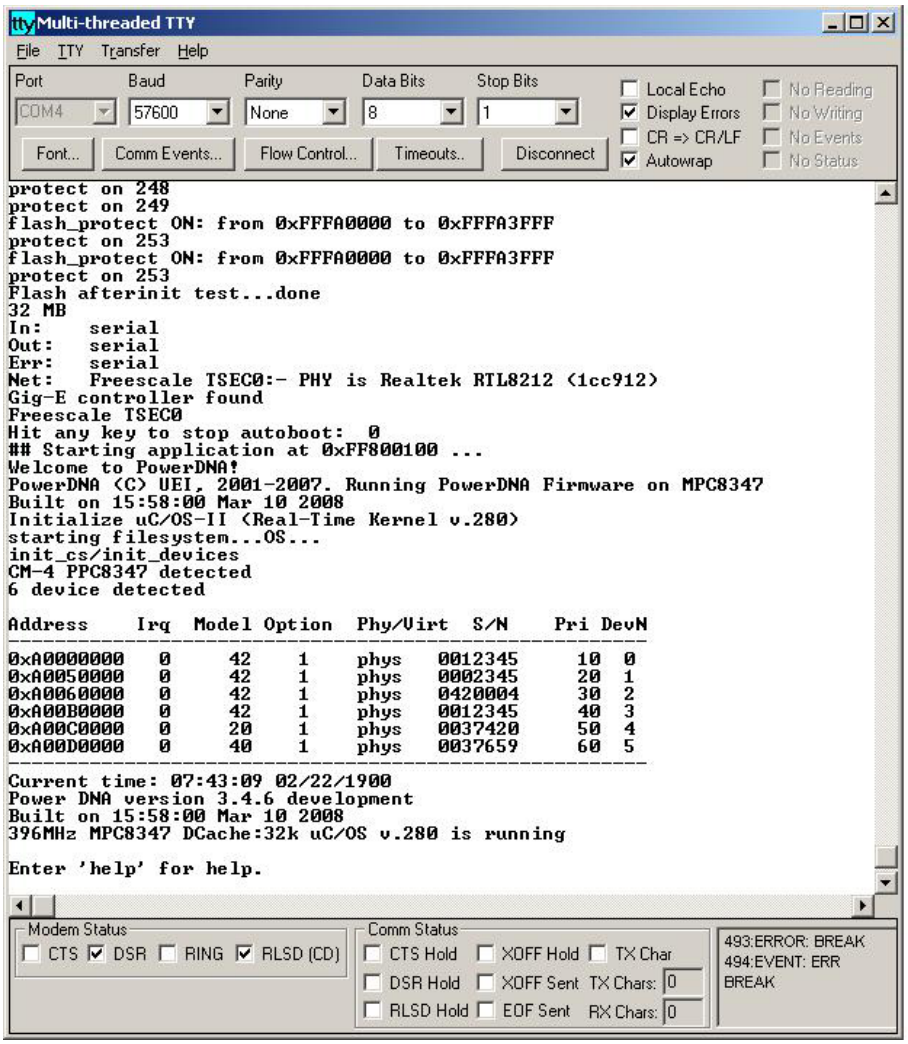


Figure 4-1. Typical MTTTY Screen

The boot process displays the model, serial number, and slot positions of boards in the rack enclosure. Type `show <CR>` to display information on system configuration, as illustrated in **Figure 4-2**.

```
DQ>show

        name: "IOM-37710"
       model: 0x3012
      serial: 0037710
        fwct: 1.2.0.0
         mac: 00:0C:94:00:93:4E
         srv: 192.168.100.2
          ip: 192.168.100.10
     gateway: 192.168.100.1
     netmask: 255.255.255.0
        mac2: 00:0C:94:F0:93:4E
        srv2: 192.168.100.102
         ip2: 192.168.100.110
    gateway2: 192.168.100.1
    netmask2: 255.255.255.0
         udp: 6334
     license: ""
    Manufactured 1/31/2008
    Calibrated 1/31/2008

DQ>
```

Figure 4-2. Show System Configuration

All parameters can be changed; most notably, the IP address, gateway, and subnet mask (netmask) configured for this system.

4.2.1 IP Addresses on the IOM

The DNR-X-1G ships with preconfigured factory default IP addresses for NIC1 and NIC2 in nonvolatile memory (usually 192.168.100.2 for NIC1 and 192.168.100.102 for NIC2). This is a static IP address; the system never retrieves its IP address from a DHCP server. This section describes why and how to change the default IP addresses.

Should you change the IP Address?

Yes, if you plan to use the DNR-X-1G on a LAN in which.

- High sampling rate is not necessary.
- Some samples can be dropped due to network congestion and collisions.
- The system should be accessible by multiple parties on the LAN.
- Multiple Cubes/systems operate (and interact) on the same network.

Alternatively, if you plan to use the system for high-speed measurements where high reliability is necessary – a direct connection between the host PC and a NIC[1] is recommended. For a direct connection, refer to “Improving Network Performance” on page 38.

How to change the IP address of the primary Ethernet port.

Both PowerDNA Explorer and a terminal-emulation program can be used to change IP addresses. Consult your system or network administrator to obtain unused IP addresses. Let’s say, for example, that your system administrator assigns you the IP 192.168.0.65 for the primary port of your IOM.

1. NIC - Network Interface Controller; a commercially available Ethernet (i.e. IEEE 802.3-2005) adapter.

To change the IP, using the terminal program, enter the following commands:

```
DQ> set ip 192.168.0.65          // Sets this system IP to 192.168.0.65
Enter user password >            // The default password is "powerdna"
powerdna

                                 // Saves the newly changed
DQ> store                        configuration
DQ> reset                        // Reboots the system for the new IP to
                                 //take effect
```

In this manner, you can set any parameters listed with the “show” command.

Connect the DNR-X-1G system to your switch with a CAT5e cable.

If you can establish communication with a DNR-CPU-1000, but later want to modify the IP address, you can also do so from within PowerDNA Explorer. After the exploratory process, go to the field where the application displays the IP address. You then enter the new IP address and hit <Return>. This action downloads the new IP address into the system’s non-volatile memory. You might also need to change the gateway and network mask to match settings on your LAN.

How to change the IP address of the secondary (diagnostic) Ethernet port.

To change the IP address of the secondary port (NIC2), use the terminal program as with the primary port, but instead use the command:

```
set ip2 aaa.bbb.ccc.ddd
```

where aaa.bbb.ccc.ddd is the new IP address for the secondary port.

Then proceed the same as with the primary port.

4.3 Improving Network Performance

To improve DNR-X-1G network performance, we recommend that instead of connecting to a company-wide network, you use separate commercially available network interface controller (NIC) cards and, where possible, set up a single dedicated mini-network for DNR-X-1G racks for both operation and diagnostics, as shown in **Figure 4-4**. As an alternative, you can configure two separate networks, one for operation and one for diagnostic purposes, as shown in **Figure 4-5**. If you do not need to connect to a company LAN and have only a single DNR-X-1G in your system, you can connect it directly to your host as shown in **Figure 4-3**.

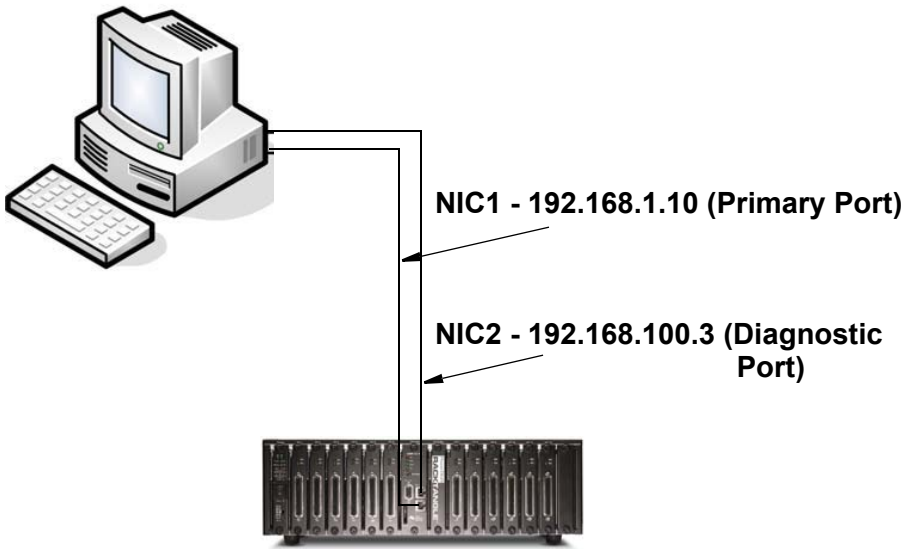


Figure 4-3. Single DNR-X-1G Direct-Connected to Host without LAN Switch

Figure 4-4 shows a two-rack single network system with a LAN switch that performs both data acquisition and diagnostic functions..

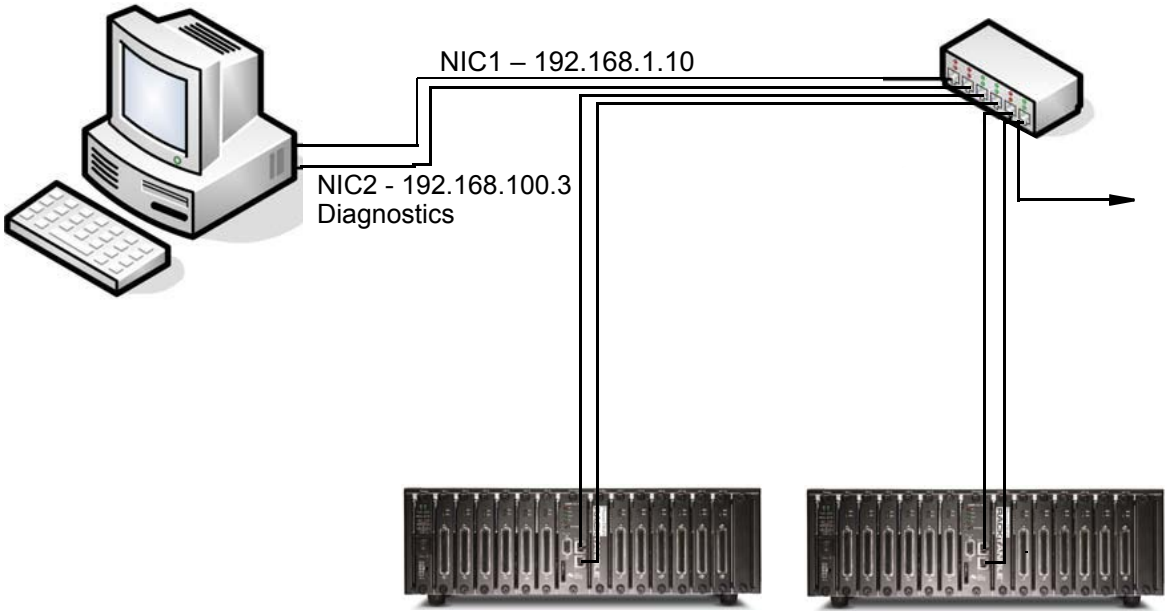


Figure 4-4. Single Network for Both Operation and Diagnostics Using Two DNR Racks and LAN Switch

Figure 4-5 shows a two-rack dual network system with two LAN switches that performs both data acquisition and diagnostic functions.

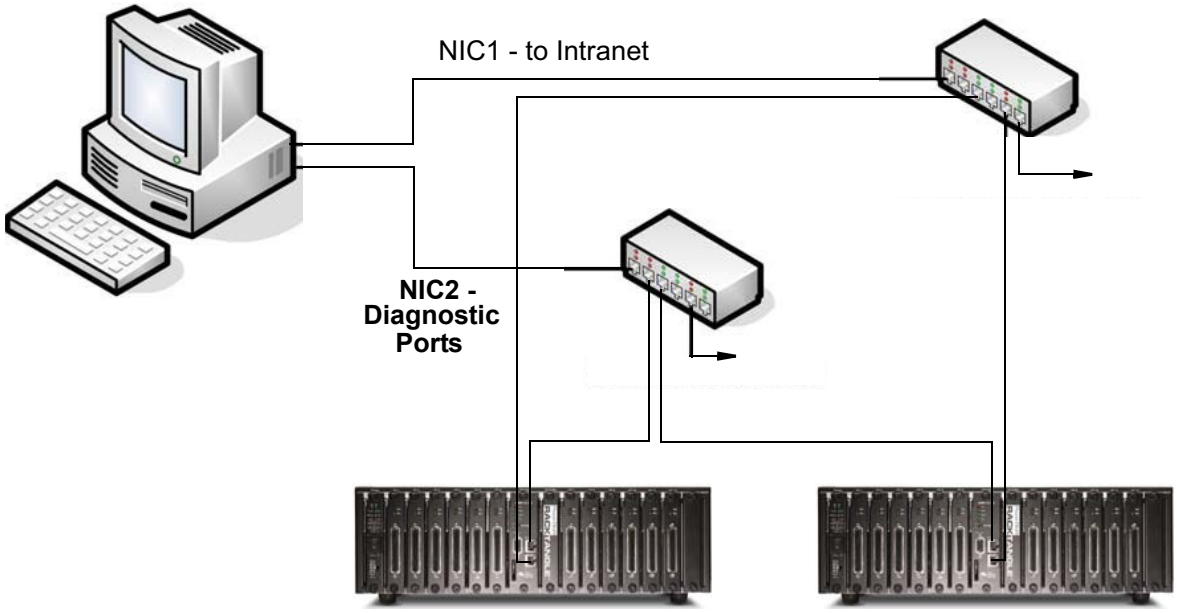


Figure 4-5. Separate Networks for Operation and Diagnostics Using Two DNR Racks and Two LAN Switches

For example, assume that your office uses a Class C network (the class intended for small networks with fewer than 256 devices) and your host is configured with a static IP or via DHCP — Dynamic Host Configuration Protocol — a protocol for assigning dynamic IP addresses to devices on a network.

STEP 1: Obtain your networking configuration by using the Command Prompt:

Start>>Programs>>(Accessories>>) Command Prompt

```
C:\> ipconfig
Ethernet adapter NIC1 - Local Area Connection:
      Connection-specific DNS Suffix  . :
      IP Address. . . . . . . . . . . . : 192.168.1.10
      Subnet Mask . . . . . . . . . . . : 255.255.255.0
      Default Gateway . . . . . . . . .: 192.168.1.1
```

Linux users can use the more verbose “ifconfig” command instead.

In the following example, the subnet range 192.168.1.0 — 192.168.1.255 is used by NIC1.

```
IP Addressing:
The range of usable addresses is defined by the IP address and subnet
maskAn IP address is a number that lies within the range of 0.0.0.0
and 255.255.255.255. Here, the IP address is 192.168.1.10.
The subnet mask indicates where an address stops. For example, a
subnet mask 255.255.255.240 has 15 usable addresses (255.255.255.255
- 255.255.255.240).
Here, the subnet is 255.255.255.0, or 255 addresses.
The subnet limits from anything.anything.anything.0 up to the max.
The usable range for 192.168.1.10/255.255.255.0 is 192.168.1.1 to
192.168.1.254 (192.168.1.0 and 192.168.1.255 are reserved for Router
and Broadcast messages).
The usable range for 192.168.0.4/255.255.0.0 is 192.168.0.1 to
192.168.255.255
The usable range for 192.168.100.2/255.255.255.0 is 192.168.100.1 to
192.168.100.254
```

```
Not every IP address from 0.0.0.0 to 255.255.255.255 is usable;
however, these three ranges of IP addresses are guaranteed open for
private use:
10.0.0.0 - 10.255.255.255
172.16.0.0 - 172.31.255.255
192.168.0.0 - 192.168.255.255
You need not use the entire set.
```

STEP 2: Install the secondary NIC card.

STEP 3: Set up a network that does not overlap the existing one.

The address space 192.168.1.0-192.168.1.255 is used. The IP address block, 192.168.2.1 to 192.168.2.255 is available and is in the private range.

Let us choose 192.168.100.1-192.168.100.255 for the PC’s secondary NIC:

```
IP: 192.168.100.3
Netmask: 255.255.255.0
Gateway:192.168.100.3
```

Using Network (Connections) in the control panel:

Start >> Programs >> Control Panel >>Network (Connections)

Right-click the adapter to bring up the Properties window.

Open the TCP/IP properties of the adapter and edit to your liking.

Refer to the Appendix at the end of this document: *"Configuring a Second Ethernet Card"* for step-by-step instructions on how to do this.
Confirm the network configuration at the Command Prompt:
Start >> Programs >> (Accessories >>) Command Prompt

```
C:\> ipconfig

Ethernet adapter NIC1 - Local Area Connection:
        Connection-specific DNS Suffix  . :
        IP Address. . . . . . . . . . . . : 192.168.1.10
        Subnet Mask . . . . . . . . . . . : 255.255.255.0
      Default Gateway . . . . . . . . .: 192.168.1.1

Ethernet adapter NIC2 - Local Area Connection 2:
        Connection-specific DNS Suffix  . :
        IP Address. . . . . . . . . . . . : 192.168.100.3
        Subnet Mask . . . . . . . . . . . : 255.255.255.0
      Default Gateway . . . . . . . . .: 192.168.100.3
```

STEP 4: Set up the DNR-X-1G system to use the same subnet, namely:

```
Cube IP: 192.168.100.2   // this is the factory default
Gateway:192.168.100.3
Netmask: 255.255.255.0
```

To do this from a serial terminal-emulation program, enter the following commands when you see the DQ command prompt:

```
DQ> set ip                  // Sets this Cube's IP address to
192.168.100.2               // 192.168.100.2
                            // Sets this Gateway to
DQ> set gateway             // 192.168.100.3
192.168.100.3               // Sets the subnet mask to 255.255.255.0
DQ> set netmask
255.255.255.0               // Saves the newly changed configuration
DQ> store                   // Reboots the system for the new IP to
DQ> reset                   take
                            // effect.
```

STEP 5: Connect the DNR-X-1G to your PC's second NIC, using a CAT5 cable. The green LEDs should light up.

STEP 6: Ping the system to make sure that it is alive.

```
C:\> ping -n 1 192.168.100.2
Pinging 192.168.100.2 with 32 bytes of data:

Reply from 192.168.100.2: bytes=32 time<1ms TTL=128
Ping statistics for 192.168.100.2:
Packets: Sent = 1, Received = 1, Lost = 0 (0% loss),
```

The above is a successful response. A “Request Timed Out” message would indicate an error.

STEP 7: The system should now be configured as shown in **Figure 4-6**.

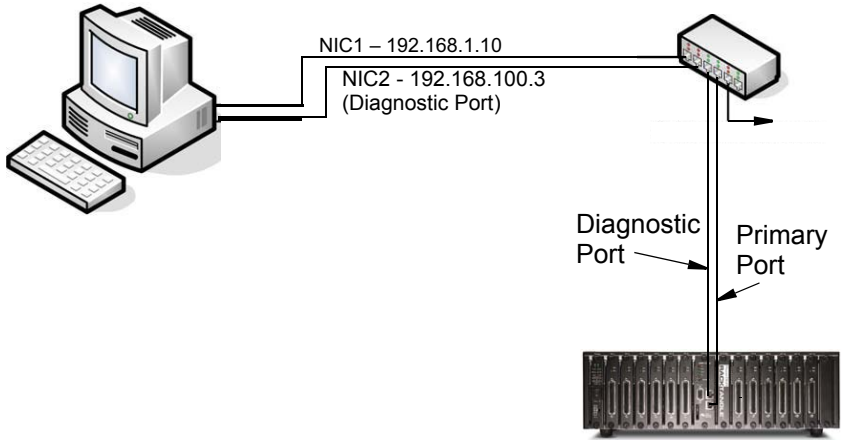


Figure 4-6. Typical Configuration for a Single DNR-X-1G with a LAN Switch

STEP 8: You may now use PowerDNA Explorer to access the system. *See* Chapter 3.

4.4.2 Trouble-shooting

The following checklist may assist you in troubleshooting a system.

☑ The PG (Power Good) LED is on: the 9-36V DC power supply is plugged into the DNR-POWER-DC Power Module panel.

☑ The green lights on NIC ports are blinking: the CAT5e cables are connected.

☑ Use the command prompt to ping <system IP> (e.g. ping 192.168.100.2)

a. Disable (temporarily) the firewall on the secondary NIC.

b. Check the secondary NIC's network settings.

c. Check the system's network settings.

– Use MTTTY and click Connect.
– Press [Enter] to display the DQ> or => prompt.
(No prompt indicates that you are not connected).
– Verify that the serial cable is firmly connected to the RS-232 port.
– Verify the settings: 57600 baud, no parity, 8 data bits, 1 stop bit.
– Try COM1, COM2, COM3 then click Connect and press `[Enter]`.

☑ Reboot the DNR-X-1G system. The start-up screen should display upon restart.

☑ If all else fails, contact UEI support at: *support@ueidaq.com*.

☑ Type "`show`" to verify the IP, Subnet Mask, and Gateway.

☑ Ensure that the computers are on a valid subnet and have valid IPs.

☑ Finally - contact UEI for support at: support@ueidaq.com.

4.5 PowerDNA Explorer Quick-Start

PowerDNA Explorer does just what its name implies: it "explores" the LAN, looking for connected PowerDNA Cubes and/or DNR-X-1G systems. Chapter 3 covers the PowerDNA Explorer in detail. This section only provides a quick-start guide.

The PowerDNA Explorer identifies DNR-X-1G systems (or Cubes) on a selected network – the discovered systems are listed on the left-hand pane of the display. Select a specific system to display pertinent hardware and firmware information. Select a board of a specific system to manipulate its inputs or outputs. In brief, this useful tool lets you verify that the system is communicating with the host and that the I/O Boards are functioning properly.

To scan the network for DNR-X-1G systems or Cubes, provide a set of addresses to scan. Do the following:

STEP 1: Select Network - Address Ranges from the menu:

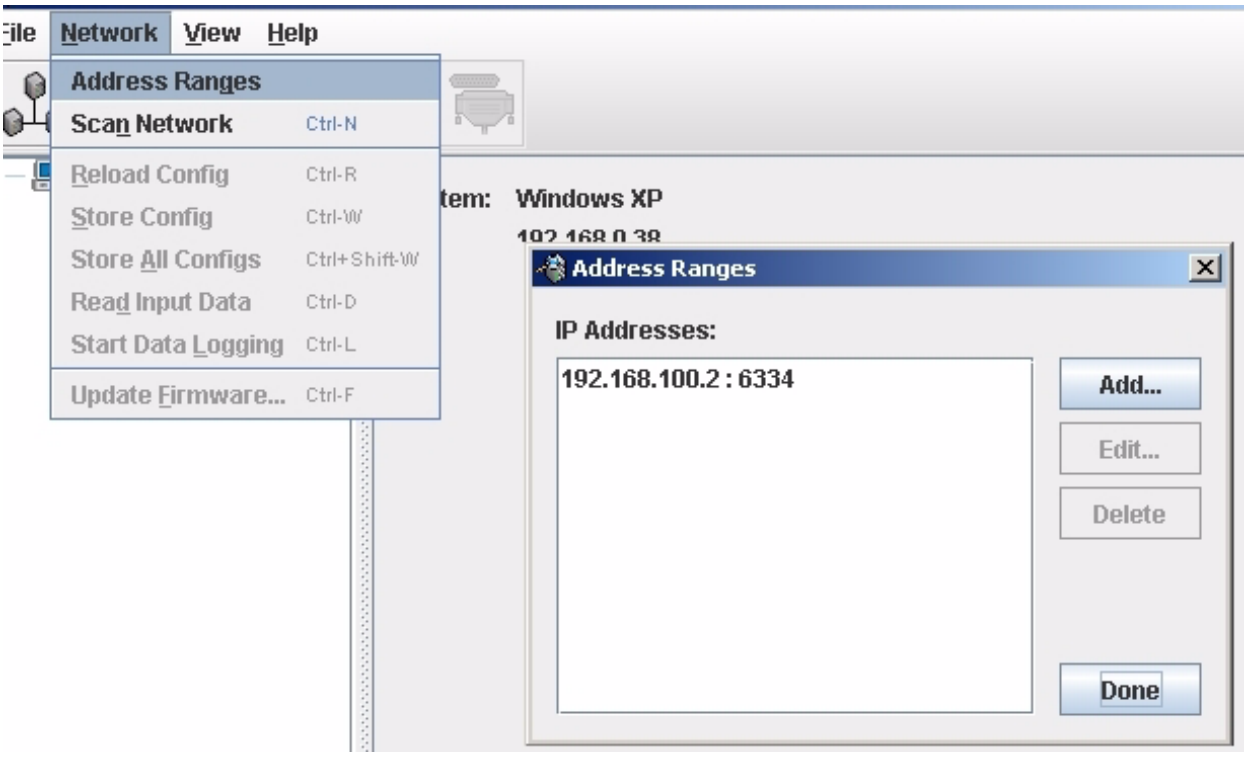


Figure 4-7. Address Ranges to be Scanned

STEP 2: Add the IP address of the PowerDNR system (e.g. 192.168.100.2); click Done.

STEP 3: Now scan the LAN for PowerDNR systems or cubes, using:

Network >> Scan Network

One or more gray icons will display in the left-hand-side of the screen. If no icons are displayed, refer to the Troubleshooting note in the previous section.

STEP 4: Double-click an icon to display its information and list the boards:

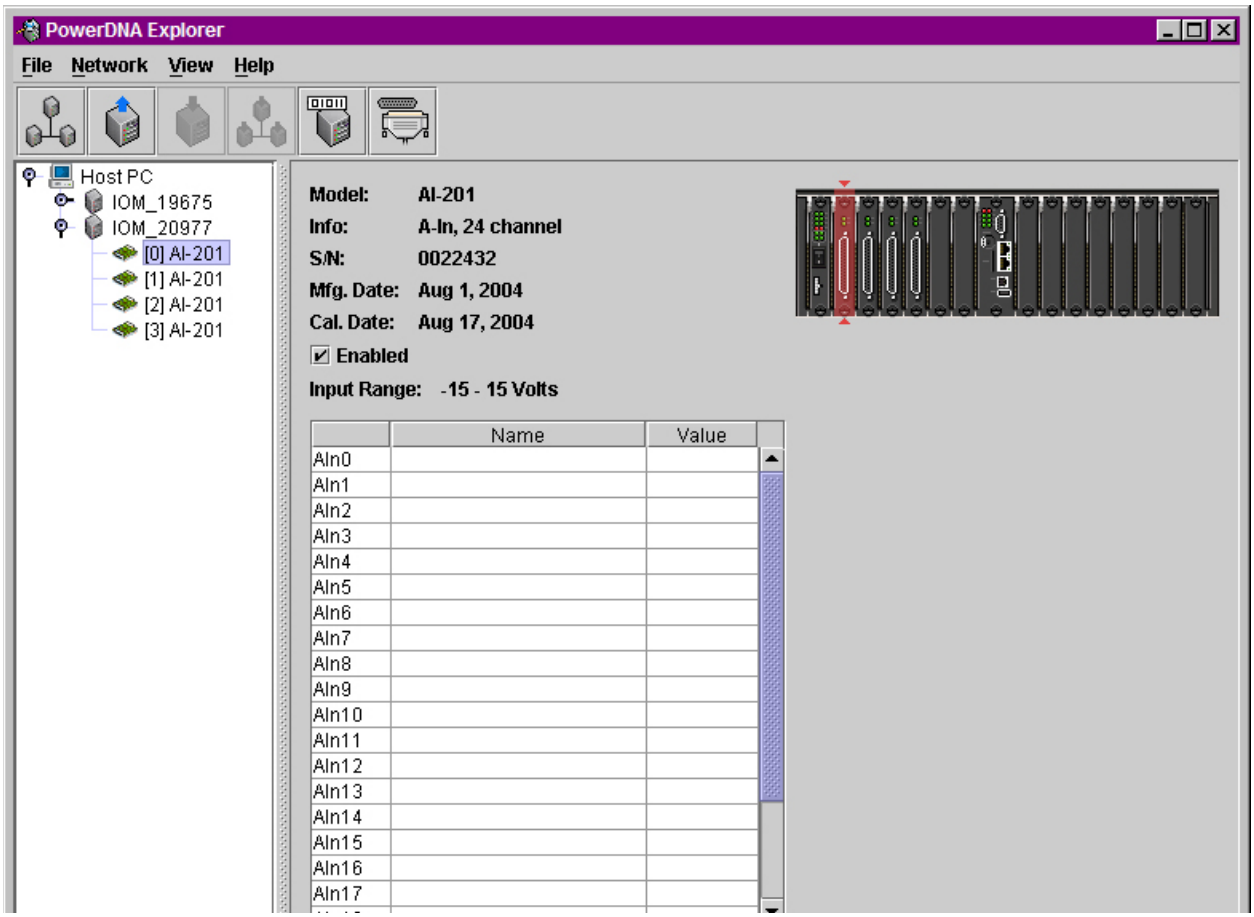


Figure 4-8. Typical Screen for Analog Input Board

The screenshot above is from the PowerDNA Explorer Demo. The "demo" is just a simulator for users without hardware – or for new users who want to explore the PowerDNA Explorer program without reading/writing to real hardware. Run this program and hover your mouse over the buttons to read the tool-tips and learn through interacting with the program.

Some quick notes:

☑ To use the I/O board, the "Enabled" check box should be set.

☑ To read from a board, click the second-to-last button: "Read Input Data"

☑ To write to the board, change the value and click the third (or fourth) button with the red arrow on top of the cube: "Store Configuration". The icon with the blue arrow above it restores the configuration.

☑ To change the IP, change the number, deselect the field, and "Store Configuration". Take care not to set the IP Address to outside of the network's configuration subnet -or- to an IP address that is currently in use, as the system will then become unreachable.

See Chapter 3, PowerDNA Explorer, for additional information and instruction.

4.5.1 Updating Firmware

Firmware in a DNR-CPU-1000 CPU module stores configuration data, along with a user application (user-app is compiled on a host PC).

Updated firmware is periodically released to introduce new features and to improve the performance of existing features. Updated releases of the firmware are bundled with the entire PowerDNA Software Suite, available for download at any time from the UEI web site (www.ueidaq.com).

CAUTION!
If you update the firmware in a DNR-CPU-1000, be sure to use the PDNA Explorer from the same release as the new firmware.

After installing the PowerDNA Software Suite, browse to the installation's Firmware directory (e.g. C:\Program Files\UEI\PowerDNA\Firmware).

The directory may contain MTTTY, updated firmware installation instructions "FirmwareInstall.html," and two sub-directories containing the firmware. Choose the sub-directory corresponding to the architecture of your system: for the DNR-X-1G, this is the **Firmware_PPC** sub-directory and the rom image file with extension MOT.

NOTE: Before updating the firmware of a system, check the version to determine which update method to use.

a. Turn on power to the DNR-POWER-DC module.

b. Connect the system to its network.

c. Start PowerDNA Explorer on the Microsoft Windows desktop from

Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer

d. Choose Network ➢ Scan Network

e. Select the DNR-X-1G icon you wish to query (by clicking the icon).

f. The version is given in the FW Ver field.

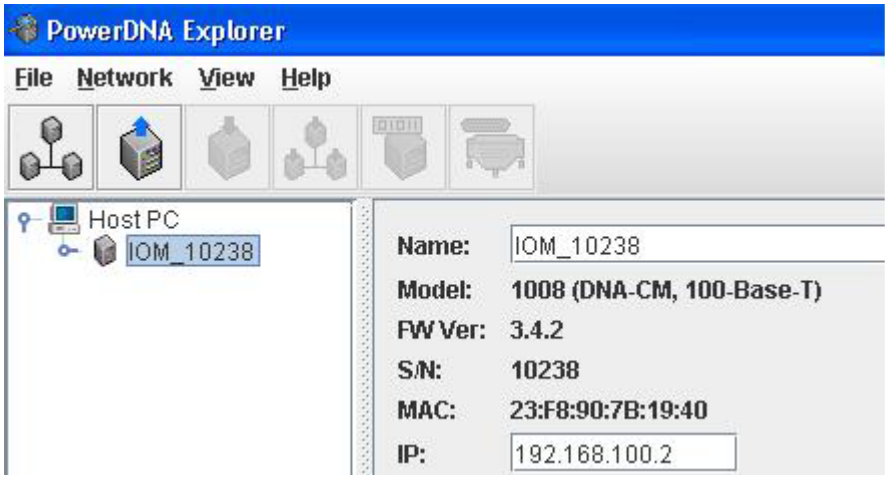


Figure 4-9. Displaying the Version of Your Firmware

If the FW Ver field has is version 2.x.x, or 3.x.x (let x be any version number), you should follow the applicable *Firmware Update Instructions* section below. For other versions of firmware (e.g. 1.x.x), refer to the user manual on the CD that accompanied your device when you purchased it.

4.5.2 Firmware Update Instructions

Before using a new release of the libraries and applications to communicate with your system, you must install the latest version of the firmware onto the DNR-CPU-1000. The version of the firmware *must* correspond to the version of the PowerDNA Software Suite — mismatched versions cause an error.

Instructions for updating the DNR-CPU-1000 via PowerDNA Explorer (over Ethernet LAN line), and over MTTTY (serial line) follow.

Firmware Update over LAN

To upload firmware with PowerDNA Explorer over LAN, do the following:

STEP 1: Turn on power on the DNR-POWER-DC module.

STEP 2: Connect the DNR-CPU-1000 module to its network.

STEP 3: Start PowerDNA Explorer on the Microsoft Windows desktop from *Start >> Programs >> UEI >> PowerDNA >> PowerDNA Explorer*

STEP 4: Choose *Network >> Scan Network*

STEP 5: Select the DNR-X-1G system to be updated.

STEP 6: Select Network >>Update Firmware…from the menu.

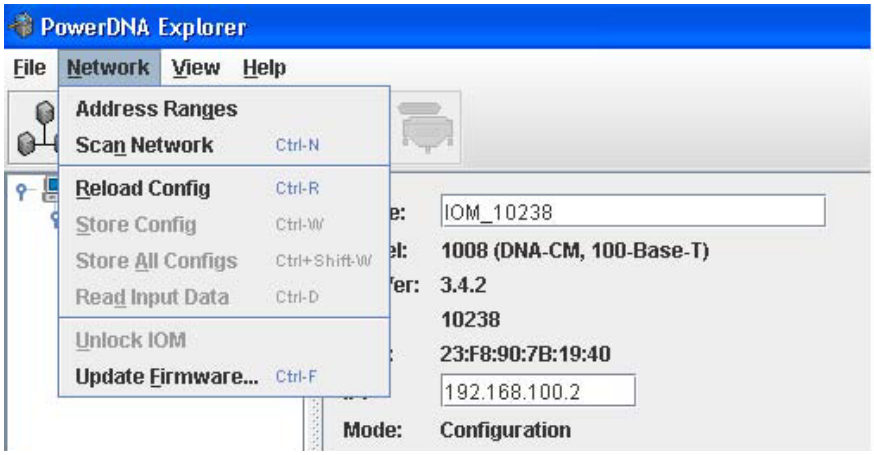


Figure 4-10. Update Firmware Menu Item

STEP 7: Click on “Yes” when you see the prompt:

`"Are you sure you want to update firmware…"`

STEP 8: Double-click on the **romimage_X.X.X.mot** (where X.X.X. is the version) file.

STEP 9: Enter the password to continue. More information about passwords can be found in the "*Interfacing to the DNR-CPU-1000 Module Using a Serial Interface*" section of this manual. DNR-X-1G systems come with the default password set to `powerdna`.

Figure 4-11. Password Dialog Box

STEP 10: Wait for the progress dialog to complete. The system will then be updated and running the new firmware.

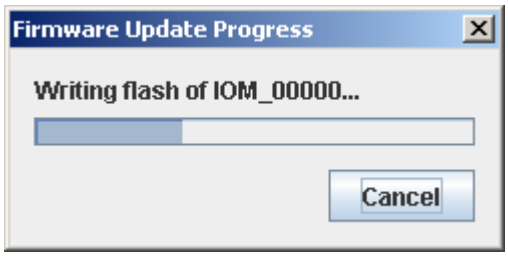


Figure 4-12. Firmware Update Progress Dialog Box

Each system is updated in three steps. First, the firmware is transferred to the system. Second, the firmware is written to the flash memory. During this step, the R/W light on the front of the cube is lit, in addition to the PG light. Third, the system is reset. During this step, the ATT, COM, and PG lights are lit, and the R/W light will turn on and off periodically. When the system is finished resetting, only the PG light is lit.

Firmware Update via Serial Port

To upload firmware over the serial port using a terminal client (MTTTY), do the following:

STEP 1: Establish communication between the PC and a DNR-CPU-1000 CPU over the serial link.

STEP 2: Use the hardware Reset switch on the front of the DNR-CPU-1000 Module to reset the CPU Module, or type: `reset all`

STEP 3: While the system is starting up again, press ESC to go into **u_boot**.

STEP 4: Type the command shown below to erase firmware download area in the Flash memory:

```
=> erase 1:192-202
=> loads rom8347.mot    // loads stores firmware into
                        //  the flash while
                        // downloading it.
```

STEP 5: Transfer the Motorola firmware file. Use *Transfer » Send File*, and select *\Program Files\UEI\PowerDNA\ Firmware_PPC\romimage_3_x_y.mot*
A progress bar will appear in the lower left corner of MTTTY, indicating progress.

STEP 6: Wait for the upload to complete (it may take a few minutes).

STEP 7: After the process finishes, enter the **f**`wjmp` command. The DNR-CPU-1000 will then be updated and running the new firmware. At this point, only the PG light on the DNR-CPU-1000 panel remains lit.

4.6 Mounting and Field Connections

You can mount the DNR-12-1G on a flat horizontal surface such as a tabletop or floor, a flat vertical surface such as a wall, or in a standard 19-inch rack. For horizontal surface mounting, use the rubber feet supplied with the standard enclosure or bolt the case directly to the surface. For mounting on a vertical wall surface, attach flanges to both ends of the enclosure with the flanges aligned flush with the rear of the enclosure; then fasten the flanges to the surface with screws or bolts. For mounting in a standard 19-inch rack, attach flanges to both ends of the enclosure with the flanges aligned flush with the front of the enclosure. Then attach the flanges to the rack with bolts.

The DNR-6-1G can be mounted in the same ways as the DNR-12-1G, except for the 19-inch rack mounting, because the DNR-6 enclosure is not as wide as the DNR-12. Refer to UEI for other accessories needed for this type of installation.

4.6.1 Physical Dimensions

The DNR-12-ENCL enclosure used in a DNR-12-1G system is compatible with Specification EIA-310-C for 19” Rack Mounting Equipment and is designed to occupy 3U units of vertical space (where 1U is 1.75”). The physical dimensions of the DNR-12-ENCL enclosure are shown below in **Figure 4-13**.

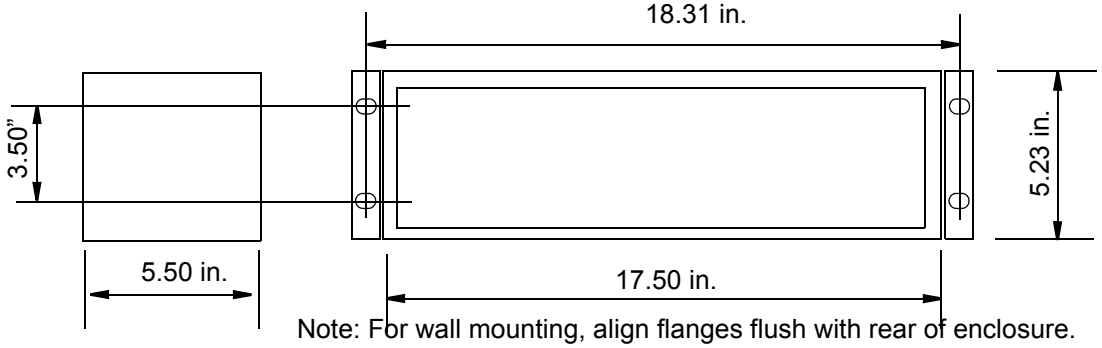
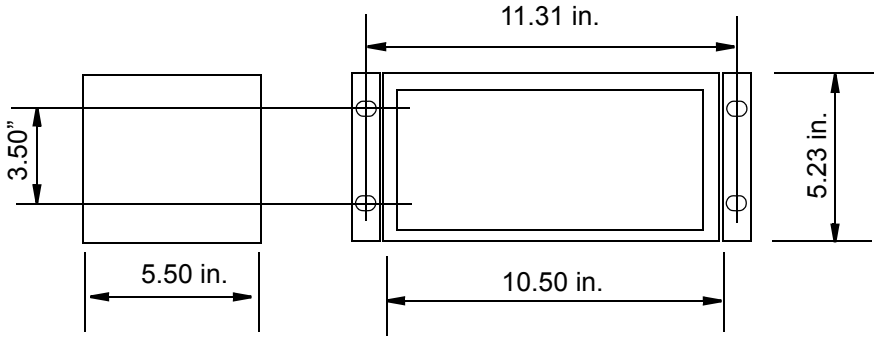

18.31 in.
3.50”
5.23 in.
5.50 in.
17.50 in.
Note: For wall mounting, align flanges flush with rear of enclosure.
For rack mounting, align flanges with front of enclosure.

Figure 4-13. Physical Dimensions of DNR-12-ENCL Enclosure

Except for the width, the DNR-6-ENCL enclosure used in a DNR-6-1G system is compatible with Specification EIA-310-C for 19” Rack Mounting Equipment and is designed to occupy 3U units of vertical space (where 1U is 1.75”). The physical dimensions of the DNR-6-ENCL enclosure are shown below in **Figure 4-14**.



Note: For wall mounting, align flanges flush with rear of enclosure. For rack mounting, refer to UEI for more information about spacer panels, flange brackets, and other accessories that may be required.

Figure 4-14. Physical Dimensions of DNR-6-ENCL Enclosure

4.7 Wiring

1000Base-T Wiring Configurations

A typical wiring configuration for a 1000Base-T network is shown in the following figure.

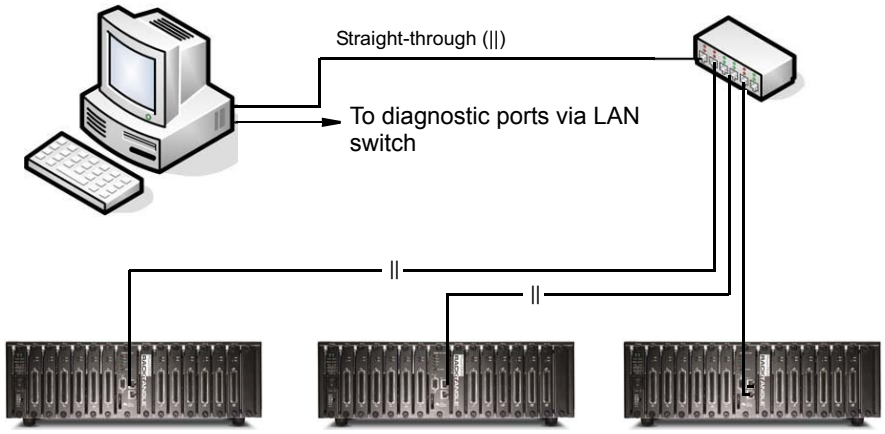


Figure 4-15. System Configuration with LAN Switch

4.8 Peripheral Terminal Panel Wiring

Refer to the applicable I/O board manuals for proper wiring to boards.

4.9 Repairing (and Upgrading) Your DNR system

DNR-X-1G systems come from the factory fully configured and calibrated. Individual modules are designed for field replacement and are not suited for field repairs. Should you encounter a problem with a DNR system, you can quickly remove and replace individual boards or other system modules in the field. You can also rearrange the locations of boards within the enclosure at any time. The system automatically senses the slot location of each board. If you want to enhance, repair, or otherwise modify a specific I/O board, however, you must send the module back to the factory or to your local distributor. This process requires that you request an RMA number from UEI before shipping. To do so, you must provide the following information:

1. Model Number of the unit
2. Serial Number of the unit
3. Reason for return
   - Calibrating the board(s)
   - Defective board for repair
   - Upgrade with additional board(s)

UEI will process the request and issue an RMA along with an estimate of the work and associated costs required to handle your request.

4.10 Configuring a NIC Port for Diagnostic Mode

The CPU Core Module has two Ethernet ports, NIC1 and NIC2. Either port can be assigned as the Main Operation Port or as a Diagnostics Port.

The main and diagnostics ports are interchangeable. The user application can open both ports independently and use separate handles to access each of them. A port becomes a diagnostics port and prevent changes in the state of the ongoing operation after it is locked -in as a diagnostics port. This allows great flexibility in IOM wiring — if either port or its cabling fails, you can use the other port as the main port.

If all layers are in configuration mode and the lock is not set, the diagnostics port functions as an equivalent of the main port. Any command that can be executed on the main port can be executed on the diagnostics port as well.

The following standard DAQBIOS commands are accessible on the diagnostics port whenever one or more layers are in operating mode:

```
DQCMD_ECHO// echo
DQCMD_RDCFG// read configuration (new)
DQCMD_RDSTS// read status
DQCMD_WRCHNL (selected)//write channel
DQCMD_RDCHNL (selected)// read channel
DQCMD_IOCTL (selected)// ioctl() - low priority command
DQCMD_SETLOCK// set/release port lock
```

Commands that are capable of changing the state of the running layers will not execute.

To switch a port into diagnostics mode, use the DQCMD_SETLOCK command, as described below:

```
int DAQLIB DqCmdSetLock (int Iom, uint8 Mode, char Password, uint32
*IP

Parameters:
int Iom// Pointer to the DQIOME structure
uint8 Mode// Function mode (lock/unlock/check/diagnostics)
char *Password// password string; ignored (and can be NULL) if Mode is
// DQSETLOCK_CHECK
uint32 *IP// returns the IP address of the locking host if Mode is
// DQSETLOCK_CHECK
<Mode> can be one of the following:
#define DQSETLOCK_LOCK0// Lock IOM to host
#define DQSETLOCK_UNLOCK1// Unlock IOM
#define DQSETLOCK_CHECK2// Get locking host IP
#define DQSETLOCK_DIAG4// Switch into diagnostics mode
```

To advance a port into diagnostics mode, call this function with the <Mode> parameter set to `DQSETLOCK_DIAG`. To return a port to normal mode, use the same function call with `DQSETLOCK_UNLOCK`.

The following table describes the possible states of both ports:

Table 4-1. Port States

Port	LOCK State	First Port (NIC1)	Second Port (NIC2)
First	DQSETLOCK_UNLOCK	Full functionality	Full functionality
	DQSETLOCK_LOCK	Full functionality, locked to the host	All but state change functions
	DQSETLOCK_DIAG	Diagnostic functionality only	Full functionality
Second	DQSETLOCK_UNLOCK	Full functionality	Full functionality
	DQSETLOCK_LOCK	All but state change functions	Full functionality, locked to the host
	DQSETLOCK_DIAG	Full functionality	Diagnostics functionality only

DQCMD_ECHO

This command returns information about the layer(s) installed. Use of this command is described in the API manual.

DQCMD_RDCFG

This command returns the current configuration of the specified layer(s):

```
int DAQLIB DqCmdReadCfg(int Iom, DQRDCFG pDQRdCfg[], uint32 maxsize,
uint32* entries)

int Iom// a pointer to the DQIOME structure
DQRDCFGpDQRdCfg[]// structure that contains layer configuration
uint32 maxsize// number of DQRDCFG structures passed
uint32* entries// number of DQRDCFG structures returned
```

```
typedef struct (
uint8DEV;// device (host fills this field)
uint8 ss;// subsystem (host)
uint32 status;// device status (device returns following fields)
uine32 cfg;// configuration, including clocks
uint32 rate;// clock divider in 15.5ns intervals
uint32 clsize;// size of the channel list
uint32 cl[];// channel list - variable size
) DQRDCFG, *pDQRDCFG;
```

Note: Use device !=0x80 to indicate that this is the last device in the list.

DQCMD_RDSTS

This command returns the status of the IOM and each and every layer in the stack (upon request):

```
int DAQLIB DqCmdReadStatus (int Iom, uint8 *DeviceNum, uint32
*Entries, uint32 *Status, uint32 *StatusSize)

Parameters:
int Iom// A pointer to the DQIOME structure
unit8 *DeviceNum// Array of layer numbers to retrieve status from
uint32 *Entries// Number of entries in DeviceNum array
uint32 *Status// Buffer to store values received from the device
uint32 *StatusSize// Size of buffer, in 32-bit chunks. Returns number
of
// 32-bit values copied into Status
```

There are special device numbers to access status of various layers:

`OxFE` – returns IOM status and status of all layers (note that each layer status is expressed as four 32-bit words. Thus, the maximum size of status packets is (4 + 14*4)*sizeof(uint32) = 240 bytes.

`0x7F` – returns IOM status only (four bytes)

`0x0 . . .0xE` – returns status of one of the layers

The status for each layer consists of four 32-bit words, as follows:

```
/* status offsets into devob].status array */
#defineSTS_STATE(0)// state of the layer
#define STS_POST(1)// post status
@define STS_FW(2)// firmware status
#define STS_LOGIC(3)// logic status
```

The first word is the state of the layer – what mode of operation it is in, and the lower 8-bits of the timestamp. If the 10us timestamp does not change after each call, the logic is in the inoperative state, as:

```
/* state flags */
#define STS_STATE_TS_SH8
#define STS_STATE_TS_SH_INS(S,TS) ((S & 0xffff00ff)|((TS<<8) &
0xff00))
```

```
#define STS_STATE_STICKY(0)
```

The second word describes the status of the layer. It is written when the layer enters initialization mode and remains unchanged until the next reboot. STS_POST_SDCARD_FAILED, STS_POST_DC24 and STS_POST_DCCORE can be changed during operation if the corresponding failure occurs.

```
/* POST status flags */
#define STS_POST_MEM_FAIL (1L<<0)// Memory test failed
#define STS_POST_EEPROM_FAIL(1L<<1)// EEPROM read failed
#define STS_POST_LAYER_FAILED(1L<<2)// Layer failure
#define STS_POST_FLASH_FAILED(1L<<3)// Flash checksum error
#define STS_POST_SDCARD_FAILED(1L<<4)// SD card is not present
#define STS_POST_DC24(1L<<5)// DC->24 layer failed
#define STS_POST_DCCORE(1L<<6)// Core voltage problem
#define STS_POST_BUSTEST_FAILED(1L<<7)// Bus test failed (hwtest.c)
#define STS_POST_BUSFAIL_DATA(1L<<8)// Bus test failed on data tst
#define STS_POST_BUSFAIL_ADDR(1L<<9)// Bus test failed on addr tst
#define STS_POST_OVERHEAT(1L<<10)// Overheat detected

#define STS_POST_STICKY
(STS_POST_MEM_FAIL|STS_POST_BUSTEST_FAILED|STS_POST_BUSFAIL_DATA|STS_
POST_BUSFAIL_ADDR
```

The third word contains the logic status flags. They are read and assembled from the various registers of the common layer interface (CLI) upon request. Not all layers implement full functionality and layers operating normally should not show any flags set.

```
/*logic status flags */
#define STS_LOGIC_DC_OOR(1UL<<0)// DC/DC out of range (IOM
//also)
#define STS_LOGIC_DC_FAILED(1UL<<1)// DC/DC failed (IOM also)
#define STS_LOGIC_TRIG_START(1UL<<2)// Trigger event started (IOM
// also)
#define STS_LOGIC_TRIG_STOP(1UL<<3)// Trigger event stopped (IOM
// also)
#define STS_LOGIC_CL0_NOT-RUNNING(1UL<<4)// Output channel list not
// running
#define STS_LOGIC_CLI_NOT_RUNNING(1UL<<5)// Input channel list not
// running
#define STS_LOGIC_CVCLK_CL0_ERR(1UL<<6)// CV clock error for CL0
#define STS_LOGIC_CVCLK_CLI_ERR(1UL<<7)// CV clock error for CLI
#define STS_LOGIC_CLCLK_CL0_ERR(1UL<<8)// CL clock error for CL0
#define STS_LOGIC_CVCLK_CLI_ERR(1UL<<9)// CL clock error for CLI

#define STS_LOGIC_NO_REPORTING(1UL<<31)// Installed logic does not
// support error reporting

#define STS_LOGIC_STICKY   (STS_LOGIC_NO_REPORTING)
```

The fourth word contains the status of the firmware. A layer operating normally does not have any flags set except STS_FW_CONFIG_DONE, which means the layer was properly configured before entering operating mode (it is cleared upon re-entering configuration mode) and STS_FW_OPER_MODE, which means that the layer switched into operating mode without any errors.

```
/* fw status flags */
#define STS_FW_CLK_OOR(1UL<<0)// Clock out of range (IOM
// also)
#define STS_FW_SYNC_ERR(1UL<<1)// Synchronization interface
// error (IOM also)
#define STS_FW_CHNL_ERR(1UL<<2)// Channel list is incorrect
#define STS_FW_BUF_SCANS_PER_INT(1UL<<3)// Buf setting error: scans/
// packet
#define STS_FW_BUF_SAMPS_PER_PKT(1UL<<4)// Buf setting error:
samples/
// packet
#define STS_FW_BUF_RING_SZ(1UL<<5)// Buf setting error: FW
// buffer ring size
#define STS_FW_BUF_PREBUF_SZ(1UL<<6)// Buf setting error: Pre-
// buffering size
#define STS_FW_BAD_CONFIG(1UL<<7)// Layer cannot operate in
// current config
#define STS_FW_BUF_OVER(1UL<<8)// Firmware buffer overrun
#define STS_FW_BUF_UNDER(1UL<<9)// Firmware buffer underrun
#define STS_FW_LYR_FIFO_OVER(1UL<<10)// Layer FIFO overrun
#define STS_FW_LYR_FIFO_UNDER(1UL<<11)// Layer FIFO underrun
#define STS_FW_EEPROM_FAIL(1UL<<12)// Layer EEPROM failed
#define STS_FW_GENERAL_FAIL(1UL<<13)// Layer general failure
#define STS_FW_ISO_TIMEOUT(1UL<<14)// Isolated part reply timeout
#define STS_FW_CLIO_FAIL(1UL<<15)// CLI or CLO counter does not
// change (or single-channel
// ops)
#define STS_FW_OUT_FAIL(1UL<<16)// Output CB tripped or over-
// current
#define STS_FW_IO_FAIL(1UL<<17)// Messaging I/O failed (5xx
// layers)
#define STS_FW_NO_MEMORY(1UL<<18//Error with memory allocation
#define STS_FW_BAD_OPER(1UL<<19)// Operation was not performed
// properly
#define STS_FW_LAYER_ERR(1UL<<20)// Layer entered operation
// successfully

#define STS_FW_CONFIG_DONE(1UL<<30)//Configuration is completed
// (no error)
#define STS_FW_OPER_MODE(1UL<<31)// Layer entered operation
// mode successfully

/* status helper macros/defines */
#define STS_FW_STICKY (STS_FW_EEPROM_FAIL|STS_FW_GEBERAL_FAIL)
```

Status bits are divided into “conditional” and “sticky”. Conditional bits are set when a condition arises; they are cleared when the error condition expires. Sticky bits are persistent once set and are cleared by reading their status.

DQCMD_IOCTL

This command is used to retrieve data from the layer. When a port is in diagnostic mode, it returns current data but cannot reprogram the channel list. The channel list is used to inform the handler the ID of the channel from which data should be retrieved.

The following functions, which rely on the DQCMD_IOCTL command for transport, are supported:

Table 4-2. List of Functions and Associated Layers

Function	Associated Layer Type(s)
DqAdv201Read	AI-201 and AI-202
DqAdv205Read	AI-205
DqAdv207Read	AI-207
DqAdv225Read	AI-225
DqAdv3xxWrite	AI-302/308 and AI-332
DqAdv40xRead	DIO-401/405/404/406
DqAdv403Read	DIO-403
DqAdv416GetAll	DIO-416 -- Voltage, current, and circuit breaker state monitoring
DqAdv432GetAll	DIO-432 -- Voltage, current, and circuit breaker state monitoring
DqAdv448Read	DIO-448
DqAdv448ReadAdc	DIO-448 -- Voltage monitoring
DqAdv501GetStatistics	SL-501and SL-508 -- Received/error counters
DqAdv566GetStatistics	ARINC-429-566 -- Received/error counters
DqAdv601Read	CT-601 -- Counters, states of input lines
DqAdv604Read	QUAD-604 -- Positions, states of input lines

Sequence of Operation

To use the diagnostic port without affecting performance of the main port, UEI recommends that you use the following sequence of operations:

1. Open main port.
2. Open diagnostics port.
3. Perform hardware reset (optional) and re-open ports, if needed.
4. Lock diagnostic port into DQSETLOCK_DIAG.
5. When operation is configured on the main port, read the status of the diagnostics port to verify that the configuration was programmed correctly.
6. Once operation on the main port is started, the diagnostics port becomes available for data retrieval.
7. Read status of the diagnostics port to make sure that all layers of interest successfully entered operating mode without error.
8. In the cycle:
    a. Retrieve the current status once a second.

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b. Check the flags for error conditions.
c. Retrieve additional data if any flags are set.

9. Stop operation and unlock diagnostics port.
10. Resume normal operation with main port.

Chapter 5 PowerDNA Explorer

The PowerDNA Explorer simplifies configuration and setup of a PowerDNR DNR-X-1G RACKtangle system under Microsoft Windows.

This section describes the various menus/screens in PowerDNA Explorer.

NOTE: The PowerDNA Explorer DEMO lets you safely explore the menus and I/O board screens without using any real hardware.

NOTE: Throughout this chapter, several screens include graphic representations of DNR-12 systems.For a DNR-6 system, each screen is the same except that it includes a photo of a DNR-6 instead of a DNR-12.

5.1 The Main Window

The Main Window of the PowerDNA Explorer is shown in **Figure 5-1**.

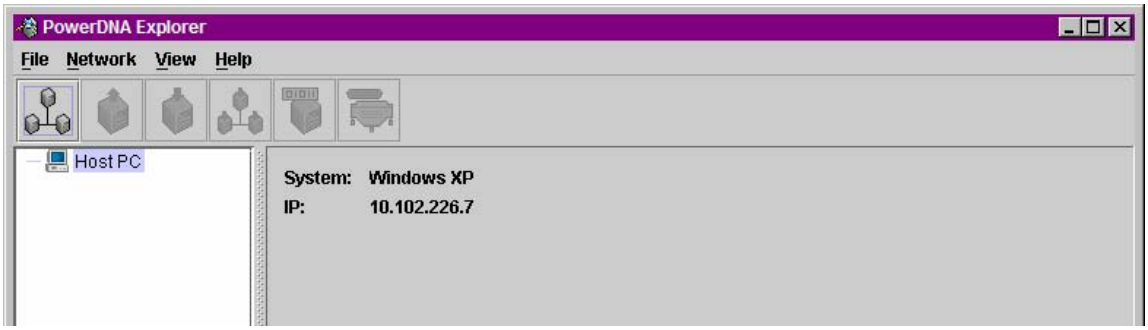


Figure 5-1. PowerDNA Explorer Main Window

The Main Window is the window you see when the PowerDNA Explorer is first launched and is where you do most of your work. It has four main parts: the Menu Bar, the Toolbar, the Device Tree, and the Settings panel.

5.2 Menu Bar

The Menu Bar contains the following menus and menu items.

5.2.1 File Menu

Preferences brings up the preferences dialog.

The preferences dialog allows you to specify the network timeout interval. This is the length of time PowerDNA Explorer will wait for response from a CPU/NIC Core Module before giving up with an error. It defaults to 100 milliseconds.

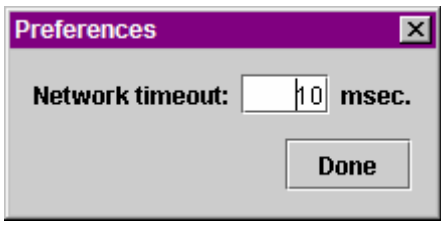


Figure 5-2. Preferences

Exit exits the application. If there are unsaved device settings changes, you are prompted for confirmation.

5.2.2 Network Menu

Address Ranges brings up the Address Ranges dialog, allowing you to specify where to scan for devices.

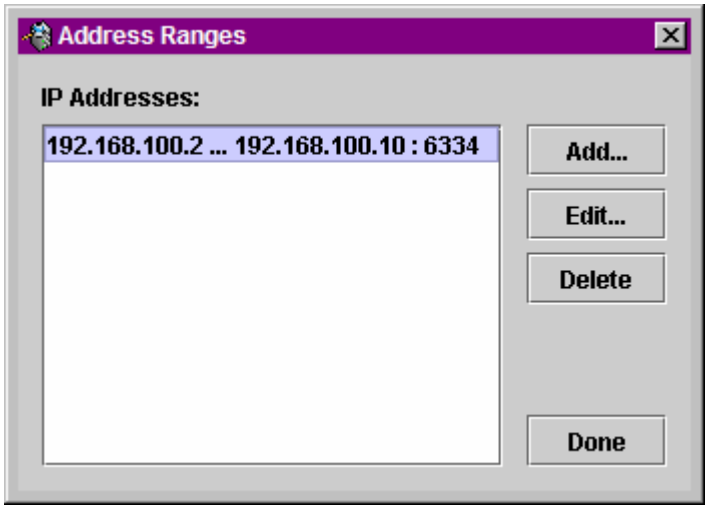


Figure 5-3. Address Ranges Dialog Box

The Address Ranges dialog allows you to specify the IP addresses and UDP port to use to find devices. You can specify individual addresses as well as address ranges. The specified items appear in a list to which you can add or delete. This list defaults to a single range item that specifies the range 192.168.100.2 ... 192.168.100.10.

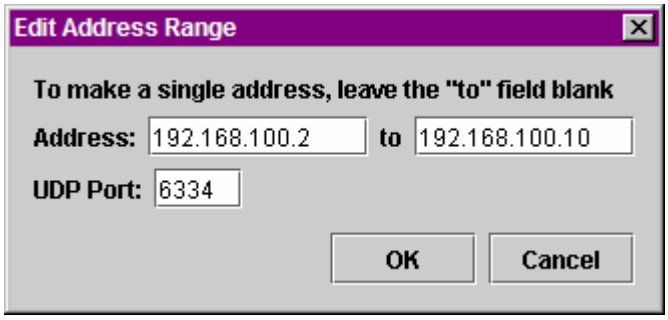


Figure 5-4. Edit Address Ranges Dialog Box

Scan Network scans the network for devices and populates the device tree. How much of the network is scanned depends on the settings in the Network Ranges dialog.

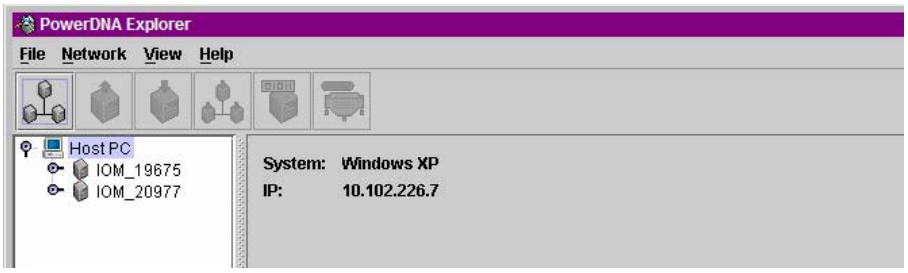


Figure 5-5. After a Network >>Scan Network

If you choose *Scan Network* when the device tree is already populated, any new devices discovered will be added to the tree. Any existing devices that are missing will be removed from the tree, unless you have made unsaved changes to such a device's configuration, in which case it will be marked in the tree as missing.

Reload Config re-reads the configuration of the current device selected in the Device Tree. If you have made changes to the settings in the settings panel for the current device, Read will replace those settings with the current settings for the device, after prompting for confirmation.

Store Config writes the changed settings for the currently selected device to the device. The button is disabled for devices that haven't been modified.

Store All Configs writes all of the changed device settings to the devices. The button is disabled if no devices have been modified.

Read Input Data is enabled when the currently selected device is an input device board. It reads the current input values to the device and causes them to be displayed in the settings panel.

Update Firmware… loads a firmware update file to all connected DNR-X-1G systems if Host PC is selected. It updates only one DNR-X-1G system when a specific unit is specified. More details about this can be found in the section *Updating Firmware in a Version 2.0 PowerDNA system*.

Note that writing certain configuration changes to a PowerDNR system running firmware 2.0.16 will bring up a password dialog box. More information about passwords can be found in the "*Interfacing to the CM module using a Serial Interface"* section of this manual. DNR-X-1G systems come with the default password set to "**powerdna**".

Figure 5-6. Password Dialog Box for "Store Config" and "Store All Configs"

Figure 5-7. Password Dialog Box for "Update Firmware . . ."

5.2.3 View Menu

Show Wiring Diagram is a friendly reminder of the connector pins for a specific board. All boards have this feature, and we display this one as an example. The wiring diagrams in PowerDNA Explorer match the wiring diagrams in this manual in the sections for each board.

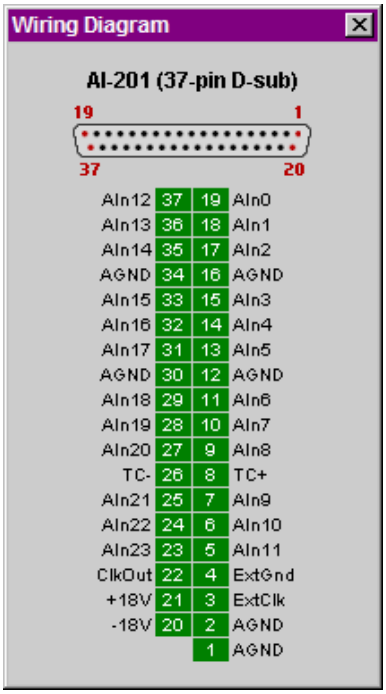


Figure 5-8. Example of a Wiring Diagram Display

5.2.4 Help Menu

About PowerDNA Explorer shows the **About ...** box, which shows the program icon, program name, version number, company name, and copyright notice.

5.2.5 Toolbar

The toolbar contains the following buttons: **Scan Network**, **Reload Config**, **Store Config**, **Store All Configs**, **Read Input Data**, and **Show Wiring Diagram**. They duplicate the functionality of the corresponding menu items as described above.

5.2.6 Device Tree

When the application is first launched, the tree contains just a root item representing the host computer. When you select Scan Network from the Network menu or the toolbar, the device tree is populated with all central controllers, IOMs, and device boards accessible from the network, as filtered through the Network Ranges dialog. Central controllers, if any, appear as children of the Host PC item. IOMs that are connected to the PC without use of a central controller also appear as direct children of the Host PC item.

Each item has an icon indicating whether it is a central controller, IOM, or board. The text label for each item is the device's model number, name, and serial number. Boards are also labeled with their position number in parentheses.

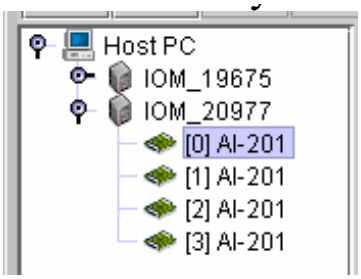


Figure 5-9. Example of the Device Tree

When an item is selected in the tree, the settings panel changes to reflect the settings for that device. The first time an item is selected, the device is queried as though you had invoked the Read command. On subsequent selections of the same item, the last settings are re-displayed. Thus, if you made changes but did not write them to the device, the changes are remembered. Invoking the Read command will re-read the device and overwrite the current settings in the settings panel.

Devices whose settings have changed, but have not been written, are displayed in bold italics in the tree to provide a visual cue. Changed devices that become missing on a subsequent invocation of Scan Network turn red in the tree. (Unchanged items that become missing are simply removed from the tree.)

5.2.7 Settings Panel

The settings panel presents a set of controls that allow you to change the settings of the device currently selected in the device tree.

5.2.7.1 IOM Settings

The settings panel has the following controls when an IOM is selected in the tree.

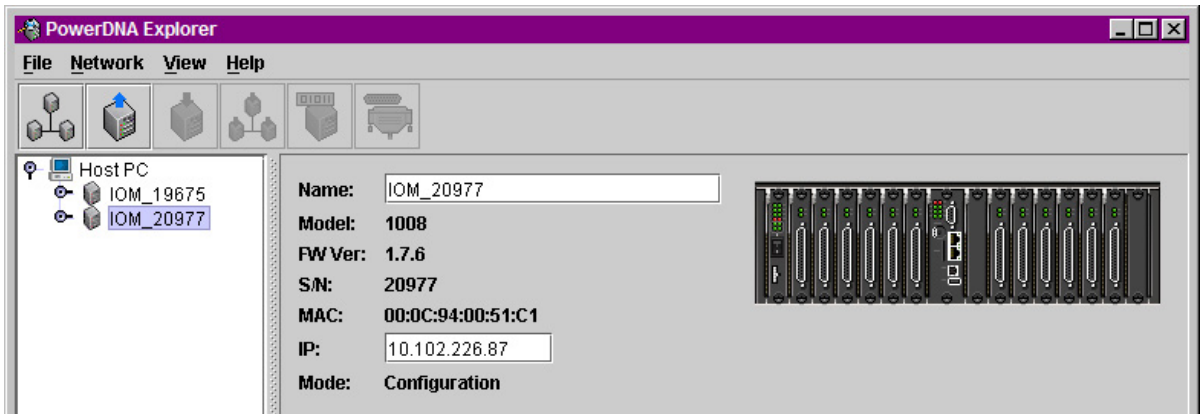


Figure 5-10. Example of IOM Settings Panel for a DNR-12-1G

Name shows the IOM name. It can be changed.

Model shows the model number of the IOM.

FW Ver shows the version of the firmware installed on the PowerDNA cube.

S/N shows the serial number of the IOM.

MAC shows the MAC address. It cannot be changed, and thus is informational only.

IP Address shows the IP address of the IOM. It can be changed.

Mode shows the mode the IOM is in: *Initialization*, *Configuration*, *Operation*, or *Shutdown*. These modes are described in the section, *IOM Modes*.

5.2.7.2 I/O Device / Layer Settings

Figure 5-11 shows the screen for displaying I/O device settings.

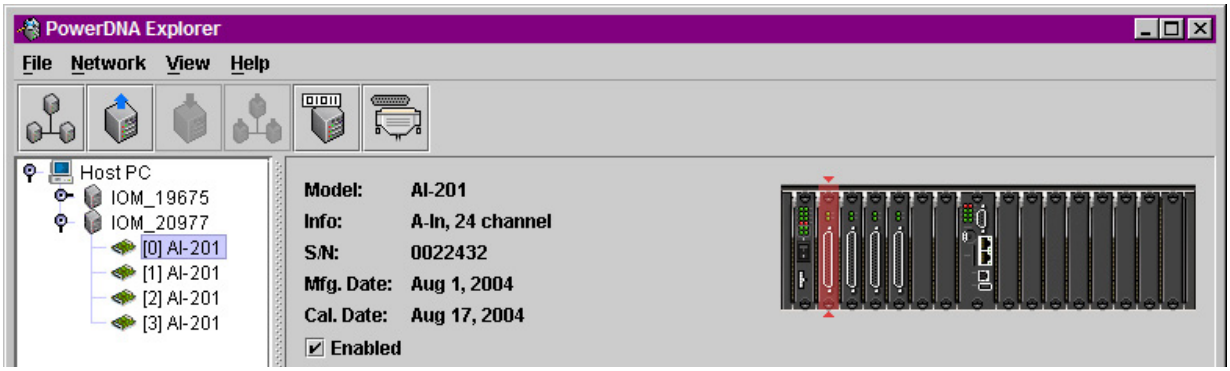


Figure 5-11. Example of I/O Device Settings

Each I/O device has the following settings.

- **Model** shows the model number of the device.
- **Info** shows some key features of the device: A for analog, D for digital, In for input, Out for output, and a number of channels available.
- **S/N** shows the device serial number.
- **Mfg. Date** shows the manufacturing date.
- **Cal. Date** shows the date of the last calibration done.
- **Enabled** is a checkbox which, when unchecked, excludes the device from configuration. The device is excluded from the Store All Configs command, and the Reload Config command is disabled. Also, the device appears gray in the tree. All devices are enabled by default.

- Select *Network >>Read Input Data* to update the Value column of any module, as shown below:

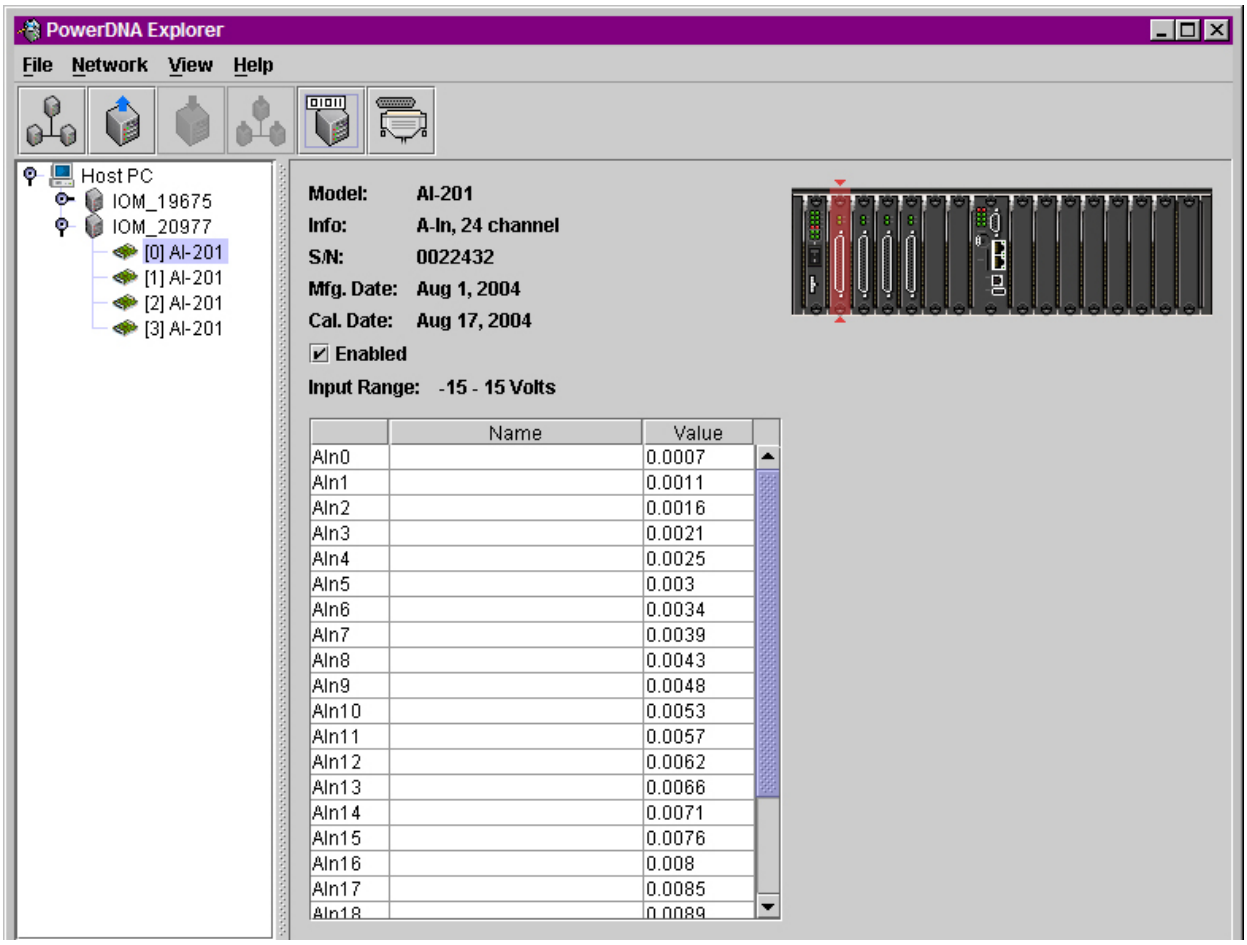


Figure 5-12. Screen from Network >> Read Input Data

At the screen shown above, you can add/edit channel names. After editing names, choose *Network >> Store Config* to save changes to the module. This is true for all modules.

Also, if you have changed a configuration value, but have not chosen *Network >> Store Config* to save them, previous values can be re-read from the module, using *Network >> Reload Config*.

AI-205 and AI-225 module screens are same as the AI-201 module, but with different input ranges and number of channels.

In addition, digital and analog output modules have settings specific to their module types.

5.2.8 Digital Input/ Output Module Settings

We'll use the DIO-405 as an example to start with, then show how the DI-401, DO-402 and DIO-403 are different.

NOTE: Use *Network >> Read Input Data* to see immediate input values in Input tabs. Use *Network >> Store Config* to save values to the module.

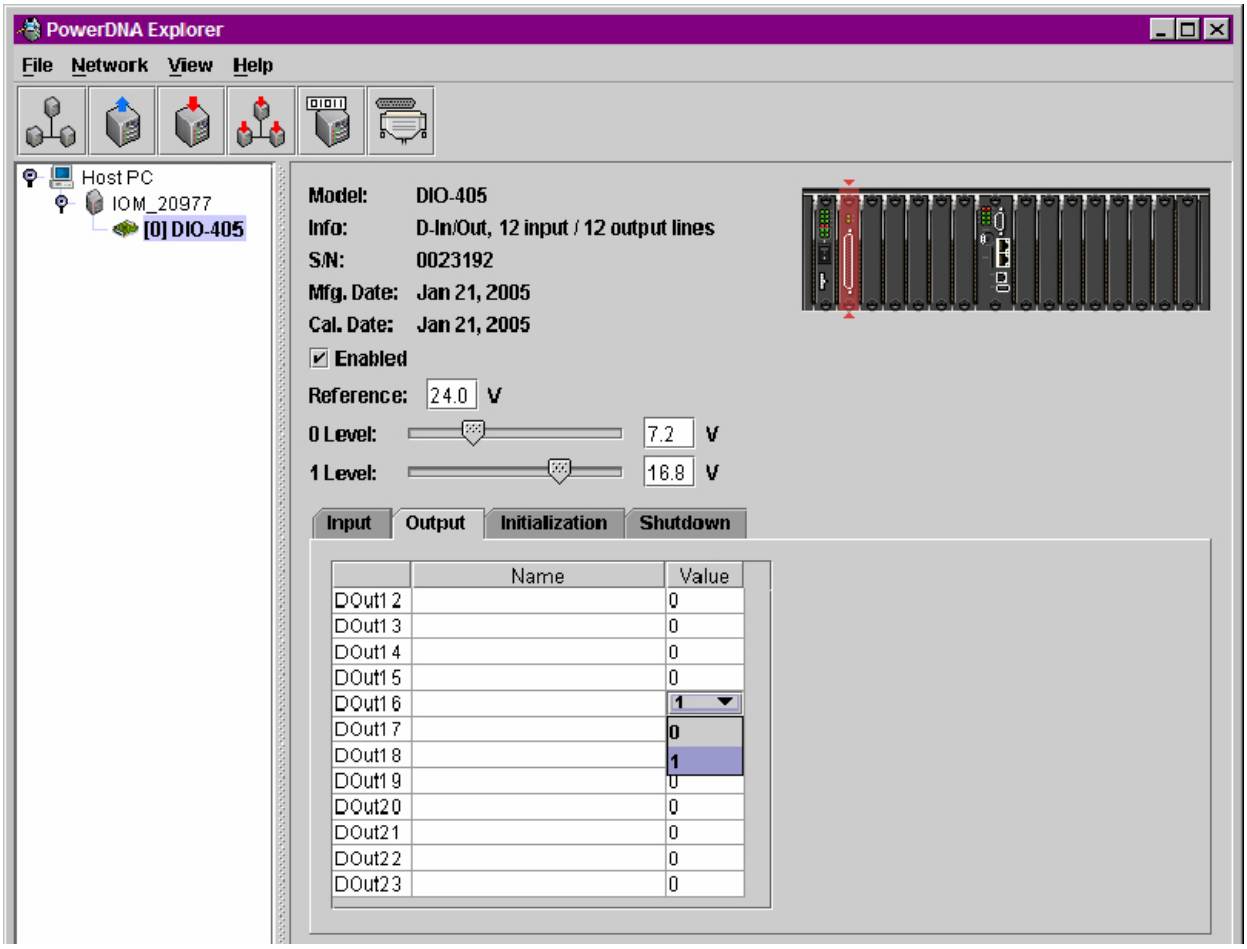


Figure 5-13. Example DIO-405 Inputs

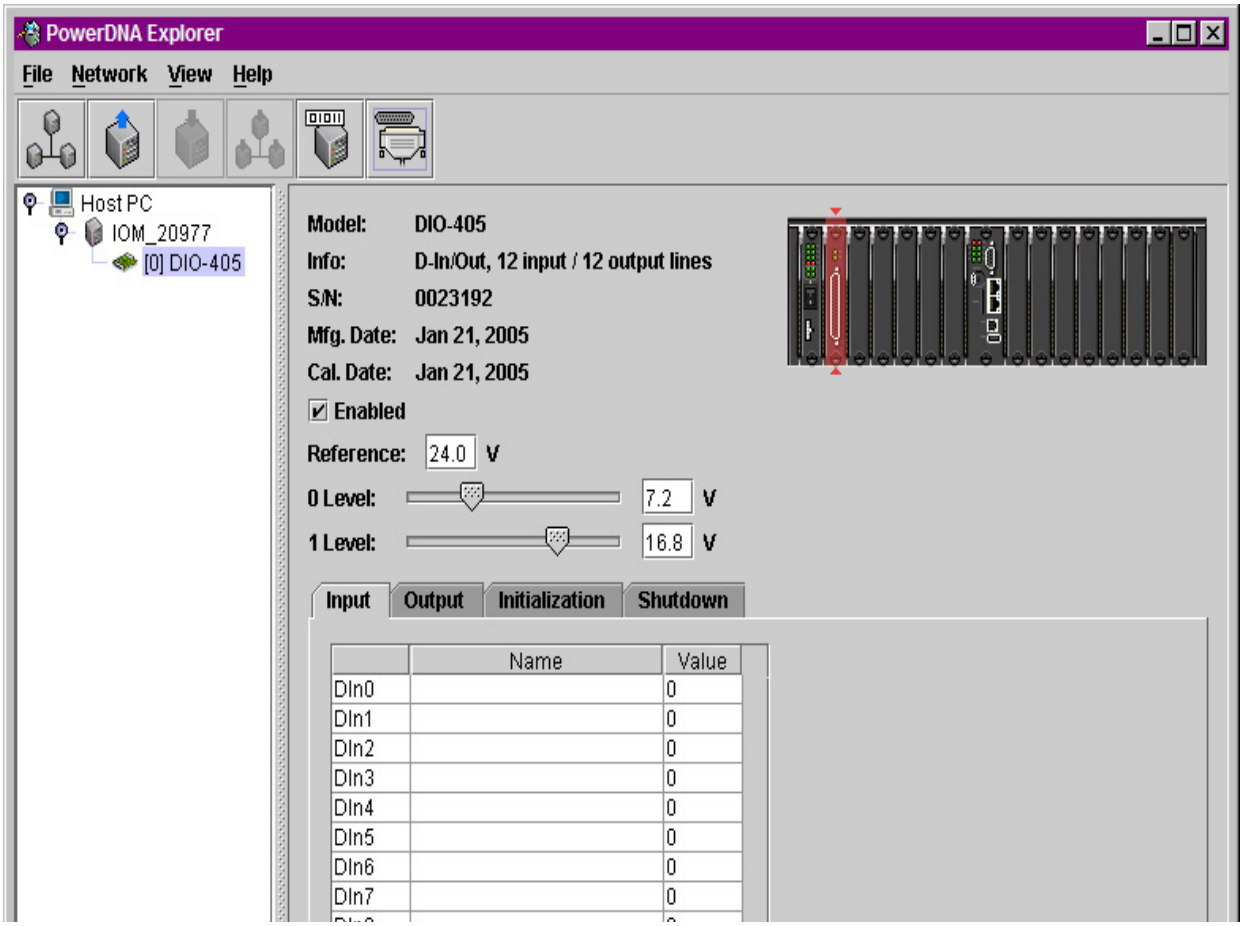


Figure 5-14. Example DIO-405 Outputs

Reference is a reference voltage.

0 level/1 level are hysteresis values described fully in the DIO-401/2/5 manuals.

Input/Output/Initialization/Shutdown tabs switch between settings for init and shutdown states, as well as operation mode configuration, and display of current data.

All tabs contain the following columns:

- The unnamed first column contains the channels.
- **Name** is a user-defined string.
- **Value** contains 0 or 1. It is a drop-down menu for output channels allowing you to select 0 or 1.

The DI-401 module just has Reference and 0 and 1 Level controls, and Input tab.

The DO-402 module just has Output, Initialization, and Shutdown tabs; no Reference value or Level sliders.

The DIO-403 module is different because it groups 8-bits at a time into ports, and three ports into two channels. For the sake of abstraction in PowerDNA Explorer, we'll call all the ports channels.

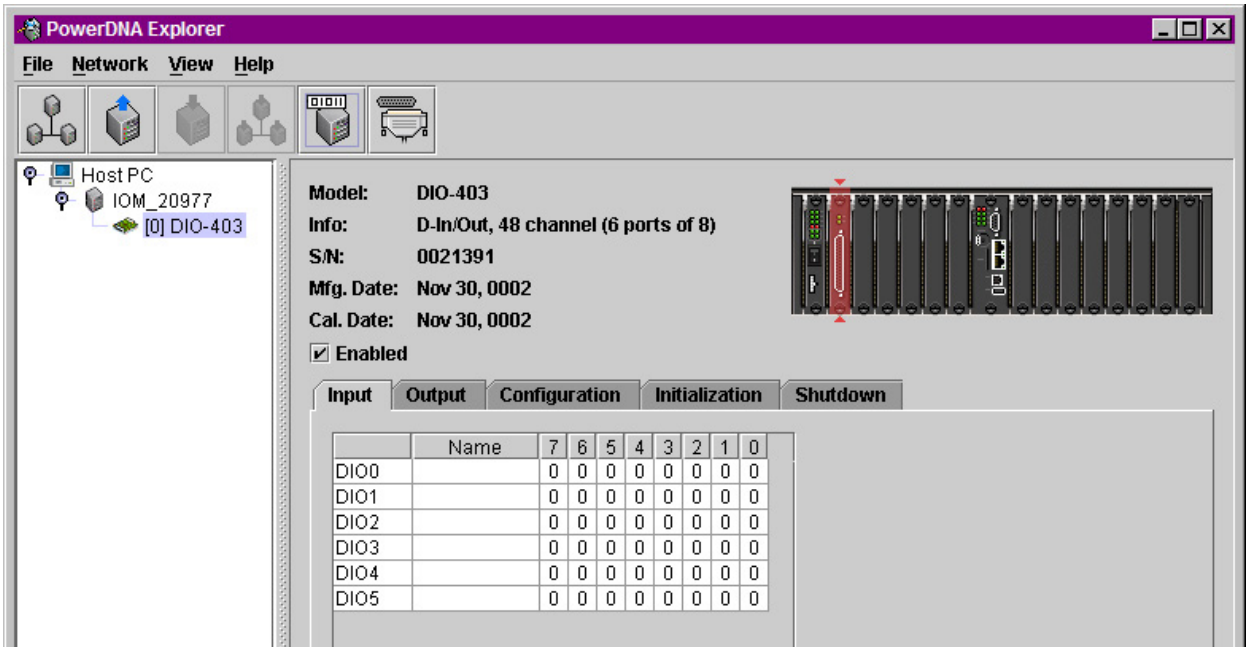

PowerDNA Explorer
File Network View Help
Host PC
IOM_20977
[0] DIO-403
Model: DIO-403
Info: D-In/Out, 48 channel (6 ports of 8)
S/N: 0021391
Mfg. Date: Nov 30, 0002
Cal. Date: Nov 30, 0002
Enabled
Input Output Configuration Initialization Shutdown
Name 7 6 5 4 3 2 1 0
DIO0 0 0 0 0 0 0 0 0
DIO1 0 0 0 0 0 0 0 0
DIO2 0 0 0 0 0 0 0 0
DIO3 0 0 0 0 0 0 0 0
DIO4 0 0 0 0 0 0 0 0
DIO5 0 0 0 0 0 0 0 0

Figure 5-15. Example of DIO-403 Inputs

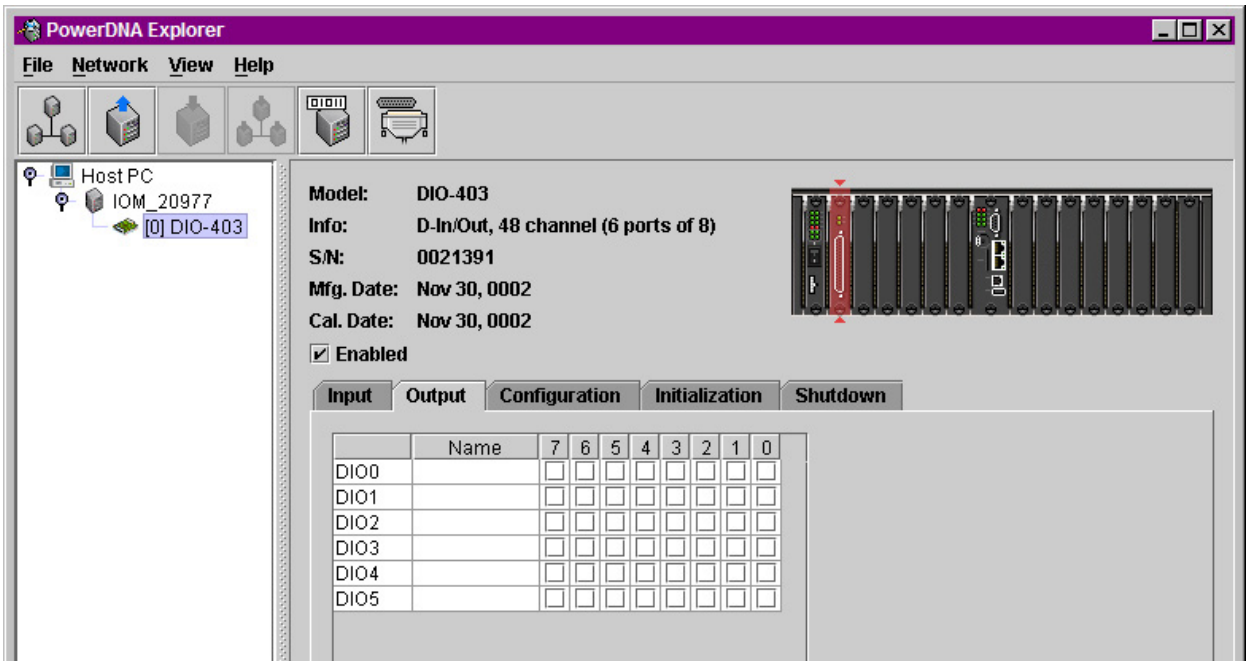


Figure 5-16. Example of DIO-403 Outputs

Input/Output/Configuration/Initialization/Shutdown tabs switch between settings for init and shutdown states, as well as operation mode configuration, and display of current data.

Input/Output tabs get/set the current input/output values. They contain the following columns:

- The unnamed first column contains the channels.
- **Name** is a user-defined string.
- **7 through 0** contain the values 0 or 1. For the output tab, they are checkmarks for output channels allowing you to select 0 (unchecked) or 1 (checked).

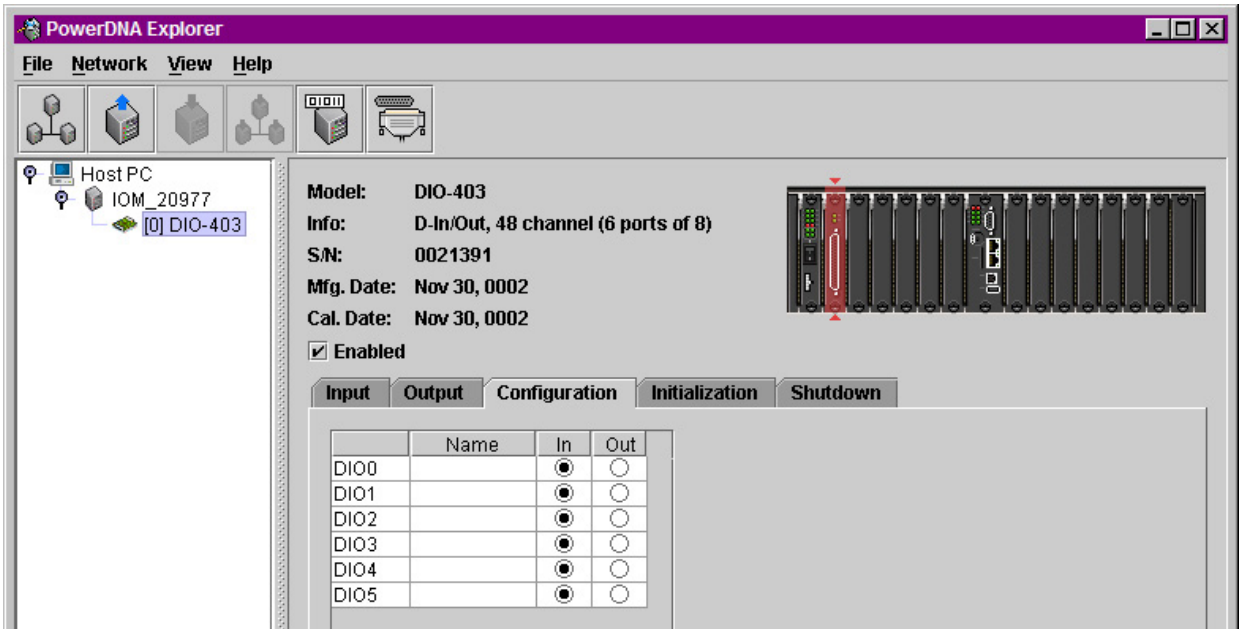


Figure 5-17. Example of DIO-403 Configuration

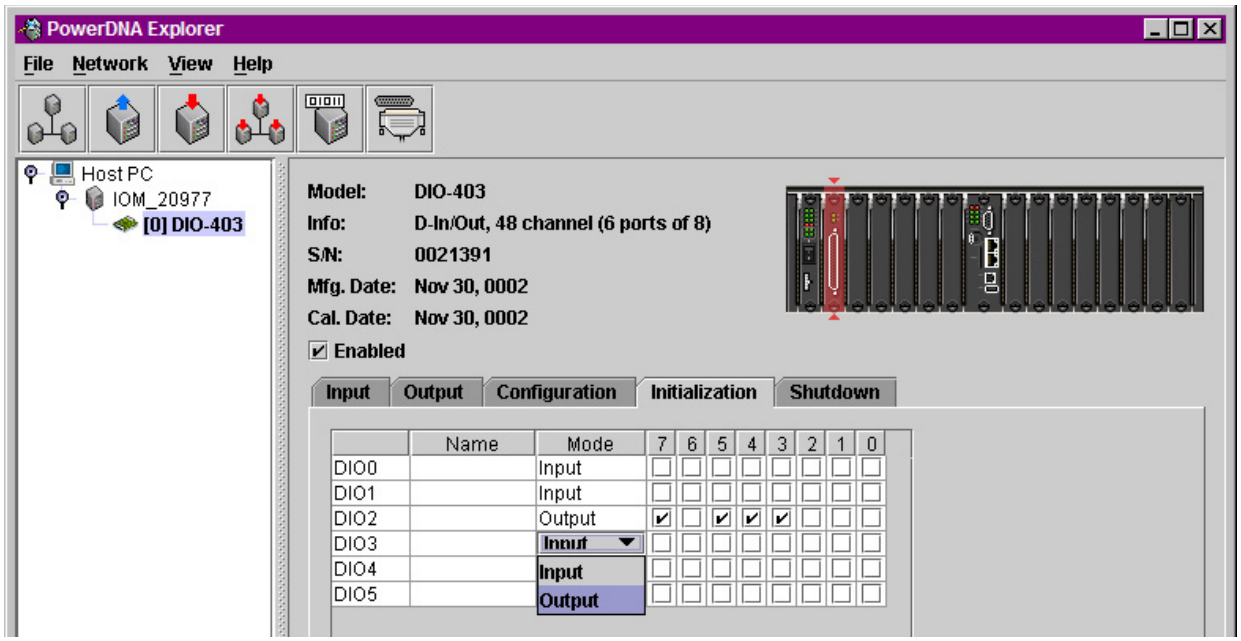


Figure 5-18. Example DIO-403 In/Outputs

Configuration tab gets/sets the current input/output directions per port. It contains the following columns:

- The unnamed first column contains the channels.
- **Name** is a user-defined string.
- **In/Out** contains toggle switches to select whether the channel is to be used for input or for output.

Initialization/Shutdown tabs allow you to set port as input or output, and set output values. They contain the following columns:

- The unnamed first column contains the channel names.
- **Name** is a user-defined string.
- **Mode** specifies whether the channel is input or output.
- **7 through 0** contain the values 0 or 1. They are checkmarks for output channels that allow you to select 0 (unchecked) or 1 (checked).

5.3 Analog Output Module Settings

We'll use the AO-302 as an example.

NOTE: Use Network >> Read Input Data to see immediate input values in Input tabs. Use Network >> Store Config to save values to the module.

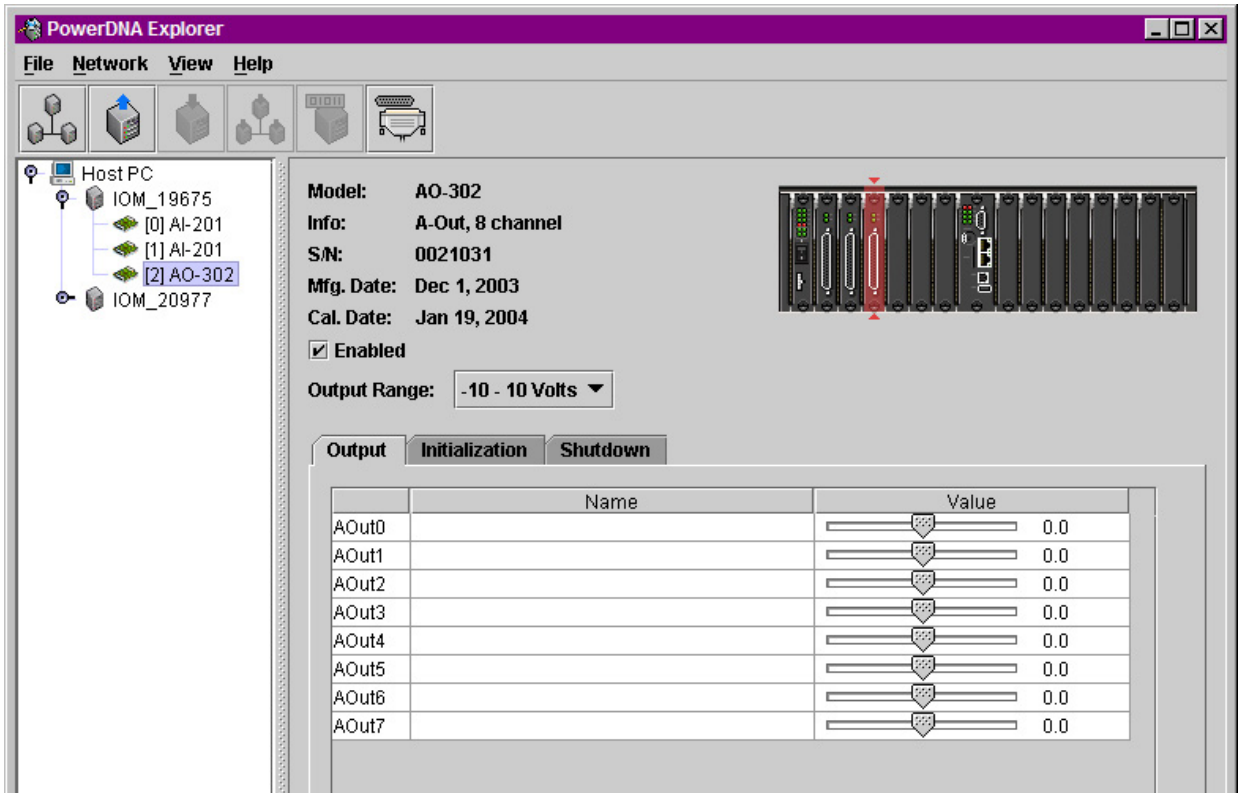


Figure 5-19. Example AO-302 Module

You can change output, initialization, and shutdown values. You can also change Output Range using the combo box, and this only affects values displayed in initialization and shutdown tabs. You can then choose *Network >> Store Config* to apply all changes to the module.

Output Range is a popup allowing you to choose between -10...0V, 0...+10V, and -10...+10V.

Output/Initialization/Shutdown tabs switch between settings for init and shutdown states, as well as operation mode configuration.

The **Output, Initialization** and **Shutdown** tabs contain the channel list table, which has the following columns:

- The unnamed first column contains the channel names.
- **Name** is a user-defined string.
- **Value** contains a slider to set the voltage to output from the channel and the numerical voltage value, which you can input directly. The actual voltage depends on the selected output range.

5.4 Analog Input Module Settings

We'll use the AI-201 as an example to start with. The AI-202 and AI-205 are similar.

NOTE: Use Network→Read Input Data to see immediate input values in Input tabs. Use Network→Store Config to save values to the module.

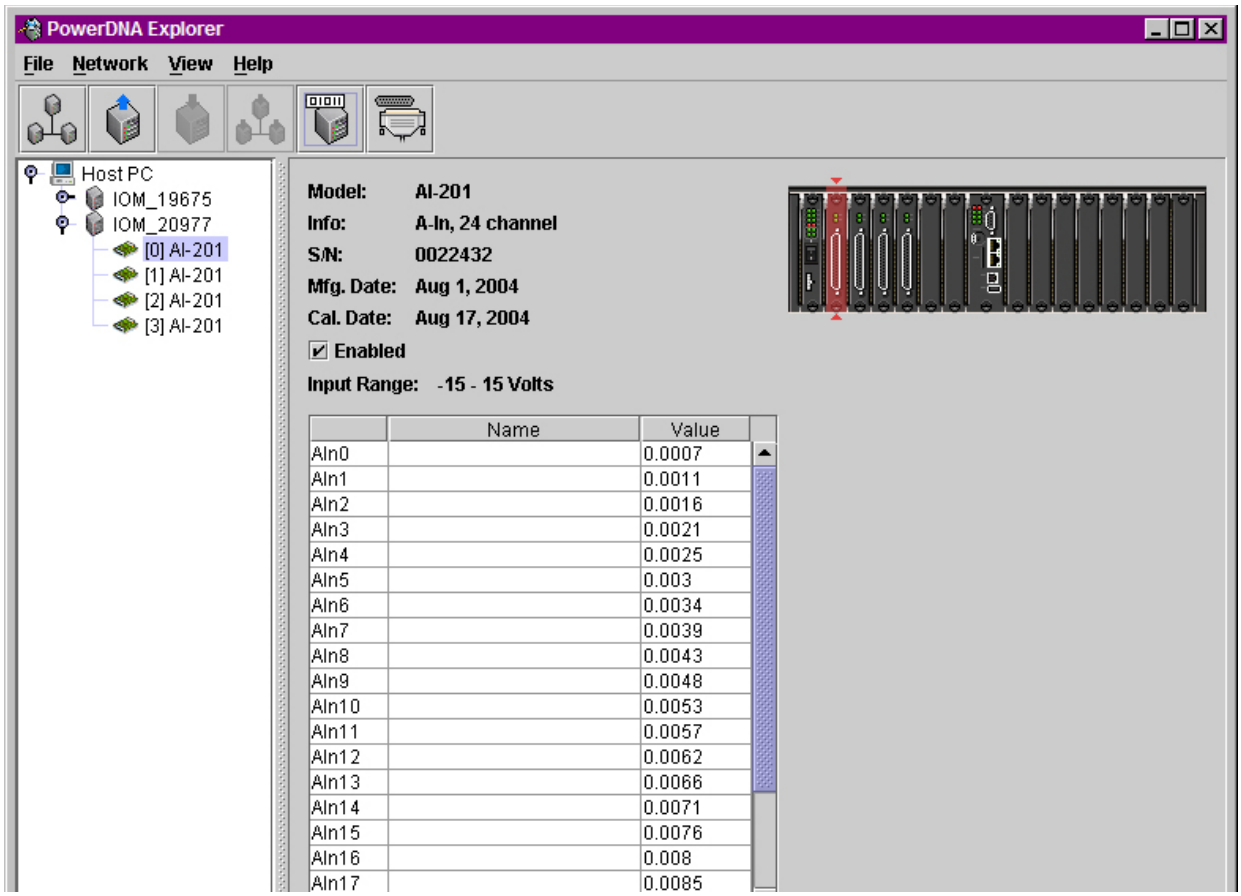


Figure 5-20. Example AI-201 Module

Input Range shows the specified input range. It cannot be changed, and thus is informational only.

The Data table contains the values currently coming into the device. The table is initially blank until you invoke Refresh Data, unless auto-refresh is activated in the preferences dialog. The table has three columns:

The unnamed first column contains the channel names.

- **Name** is a user-defined string.
- **Value** shows the current value.

5.5 Counter/ Timer Module Settings

We'll use the CT-601 as an example.

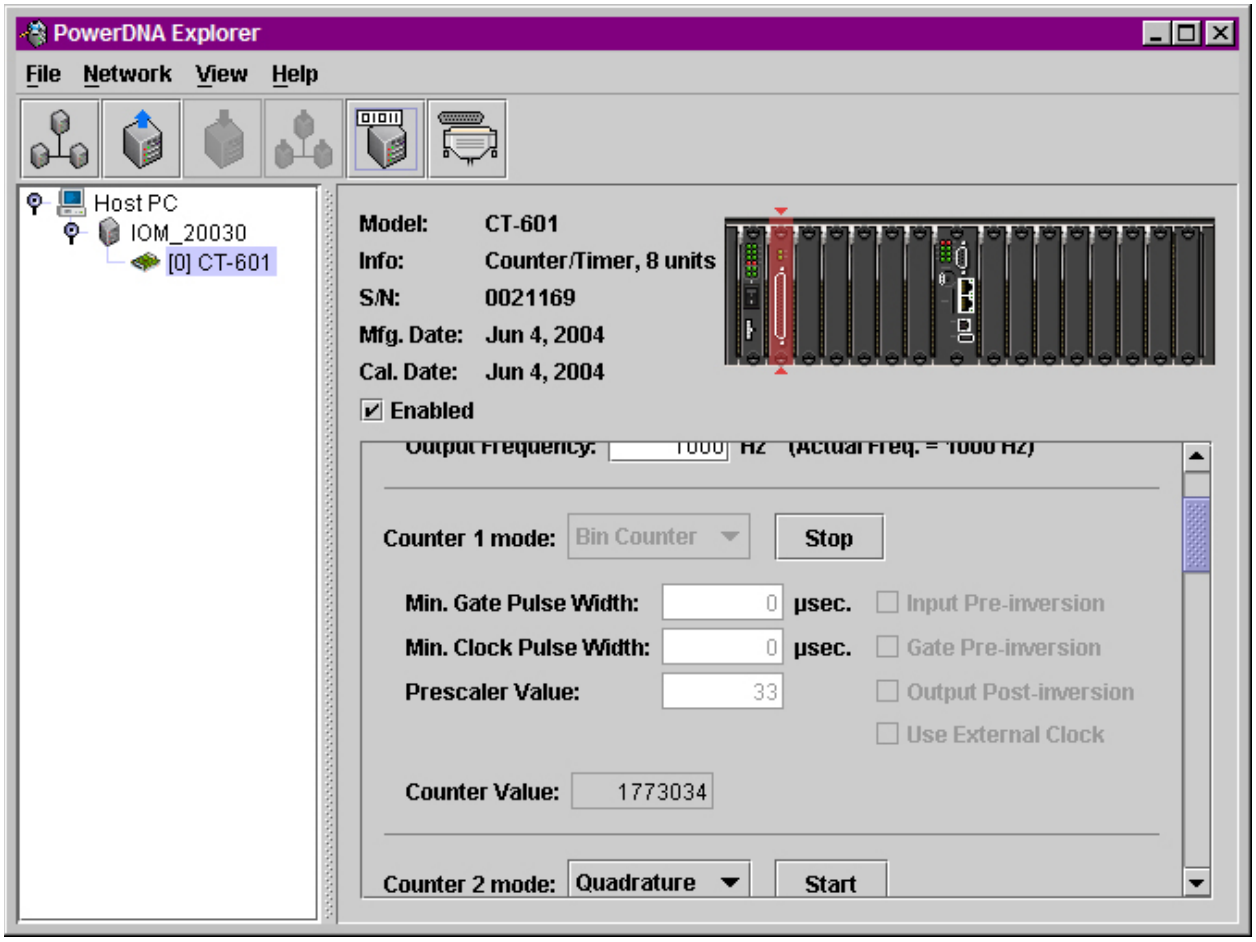


Figure 5-21. Example CT-601 Module

The CT-601 module has 8 counters. Each counter can be set to one of four different modes: Quadrature, Bin Counter, Pulse Width Modulation (PWM), or Pulse Period. When you change the mode of a counter using the mode combo box, the controls for that counter will change to those appropriate for the mode.

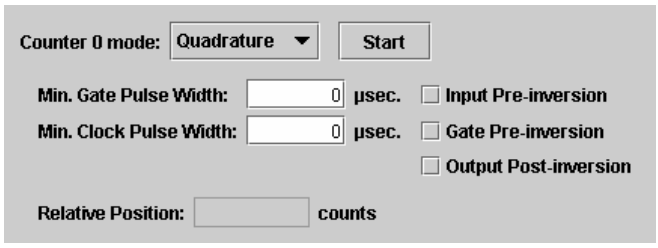


Figure 5-22. Example Quadrature Controls

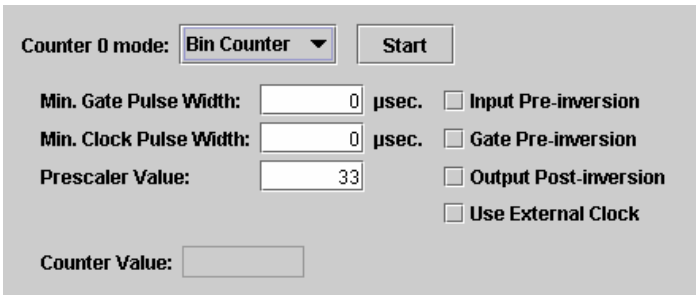
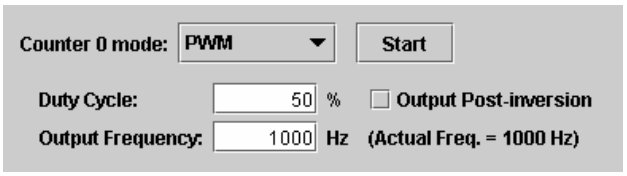


Figure 5-23. Example Bin Counter Controls



Example Pulse Width Modulation (PWM) controls

Figure 5-24. Example Pulse Width Modulation (PWM) Controls

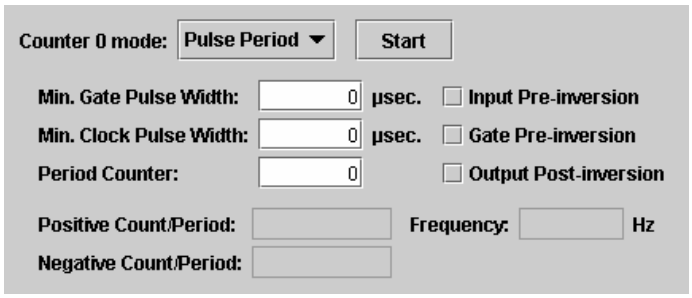


Figure 5-25. Example Pulse Period Controls

After setting the configuration for a counter, you can choose *Network→Store Config* to store the settings on the device. Clicking the Start button will also write your configuration to the module.

Clicking the Start button for a counter will start that counter on the module. The Start button will turn into a Stop button, and the other controls for that counter will become disabled until you click Stop. While the module is running, you can choose *Network→Read Input Data* to retrieve runtime values from the counter, which will display in the read-only text field(s) of the counter control panel.

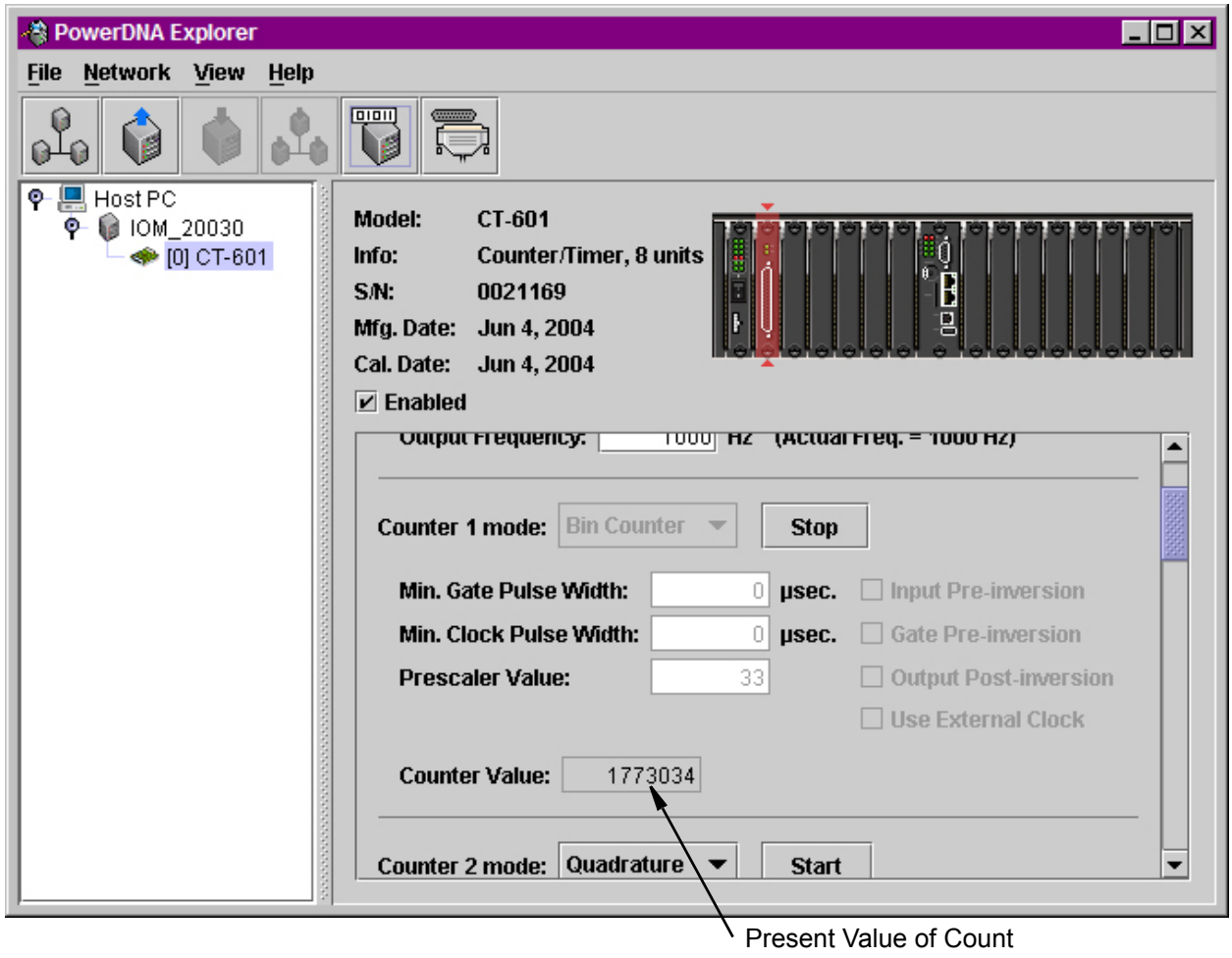


Figure 5-26. Example of Started Counter

Chapter 6 The DNR-CPU-1000 Core Module

This chapter focuses on the device architecture of the Core Module, not I/O modules.

Two slots of a DNR-X-1G *RACK*tangle™ Enclosure are occupied by the PowerDNR Core Module, called the DNR-CPU-1000.

The Core Module consists of a Freescale (formerly Motorola) MPC8347 32-bit 400 MHz CPU and peripheral devices (USB 2.0, RS-232, NIC, SD, etc) for use with a Gigabit Ethernet communication network and an internal 66 MHz 32-bit common logic interface bus. The NICs are copper (1000BaseT) interfaces. The module has an RS-232 port used for configuration and also two USB 2.0 ports (controller and slave) for general purpose use (not implemented yet). LEDs on the front panel of each module indicate the current operating status of the device.

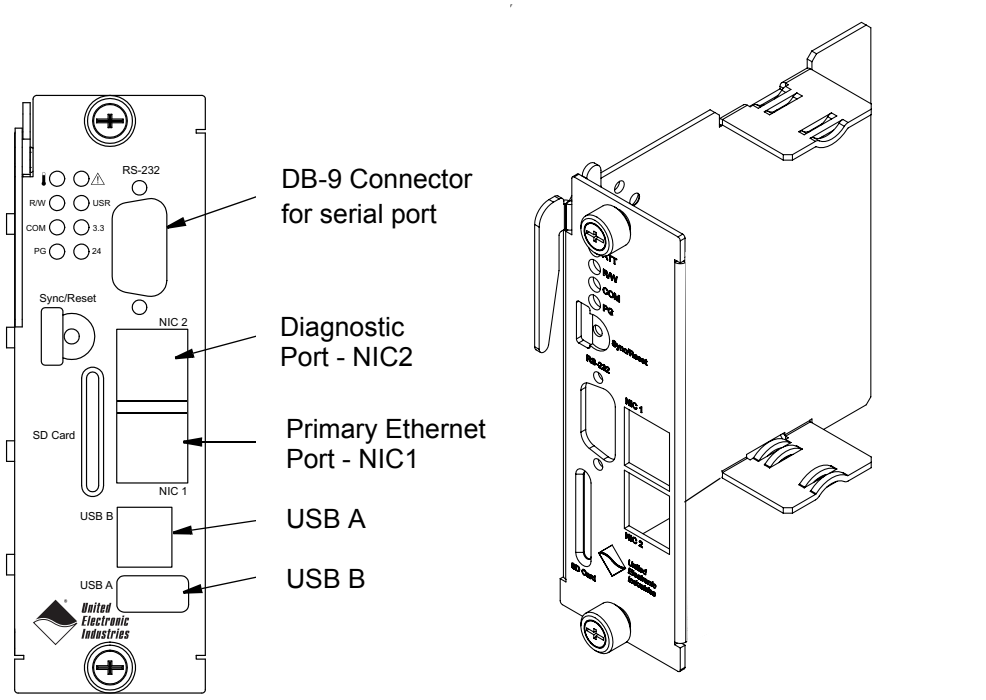


Figure 6-1. PowerDNR Core Module (CPU/NIC) – DNR-CPU-1000

6.1 Device Architecture of DNR Core Module

The DNR-CPU-1000 Core Module architecture can be represented as follows:

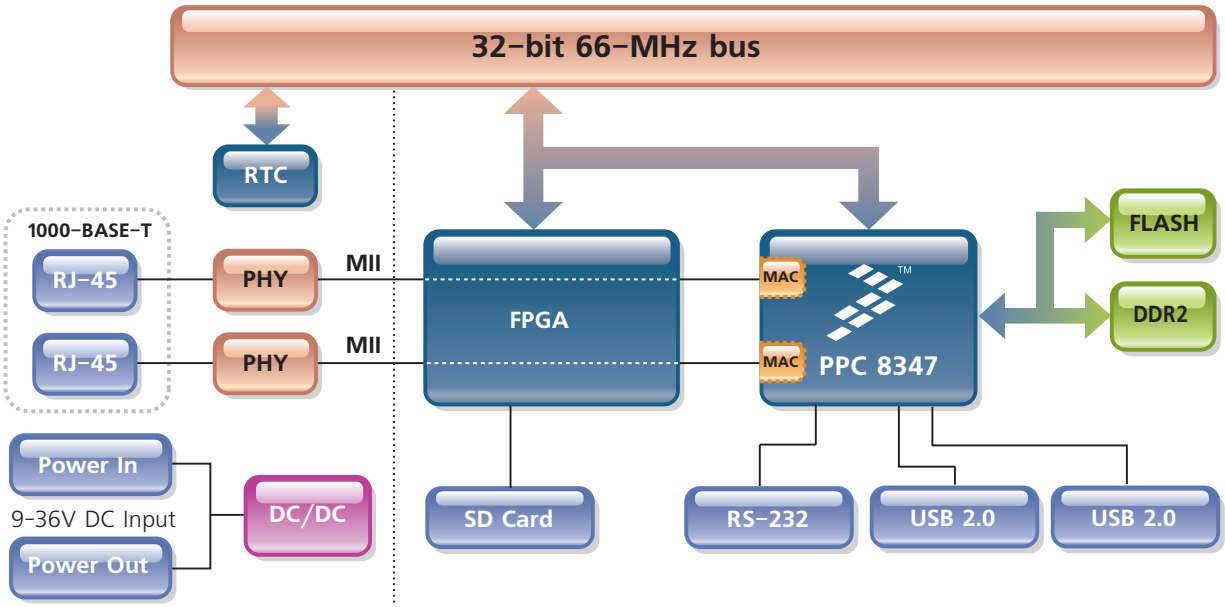


Figure 6-2. FreeScale PowerPC CPU/NIC Controller Architecture

The core of the system is a Freescale (formerly Motorola) PowerPC MPC8347 32-bit 400 MHz processor, which controls the following components:

- Primary Network Interface MII Port – NIC1
- Diagnostic Network Interface Port – NIC2
- RS-232 serial port
- UBS 2.0 dual port (Controller and Slave) (for future use)
- 32MB flash memory
- 128MB of SDRAM
- SYNC port
- Control logic
- LEDs
- SD Card Slot (Card not included)
- Watchdog timer with real-time clock (battery backed)

Not all components are available for control from the CPU. The CPU can program flash memory, set the LEDs, set up the watchdog timer, set the real-time clock and use 256 bytes of backed-up memory in the watchdog timer chip. All functions are available at the firmware level only (described in iom.c/iom.h).

6.1.1 Primary Network Interface MII Port – NIC1

This port provides communication between the DNR system and the primary LAN network.

6.1.2 Diagnostic Network Interface Port – NIC2

This port enables the user to monitor the health of the DNR system during operation, using a separate diagnostic port. This port may also be assigned as the primary Ethernet port if NIC1 is not available for use.

6.1.3 RS-232 Port

This port provides a serial communication link between the DNR-X-1G system and a standard RS-232 terminal.

6.1.4 UBS 2.0 Dual Port (Controller and Slave)

The USB A and B ports are intended for future use and are not software supported at present.

6.1.5 32MB Flash Memory

The DNR-X-1G system is provided with 32MB of flash memory.

6.1.6 128MB of SDRAM

The system is supplied with 128MB of SDRAM.

6.1.7 SYNC Port

A high-speed system to system synchronization connector permits triggers or clocks to be shared among multiple systems. Two systems may be connected together directly and larger groups may use the SYNC interface to share timing signals among many racks and systems.

The trigger and clock inputs will accept signals from standard digital logic that is powered in the range of 3.3V to 5V. The inputs also have internal pull-up resistors to an internal 5V supply, making the inputs also compatible with a low-side drive open-collector output. The Sync and trigger outputs have 5V logic levels. The sync connector's ground and 5V power connections are provided by its own isolated DC-DC converter.

6.1.8 SD Card

A slot for inserting a user-provided Secure Digital card is provided for on-board data storage. It can also store both data and Linux embedded programs using the soon-to-be-released embedded toolkit. Supports FAT12, FAT16, and FAT32 file systems.

6.1.9 LEDs

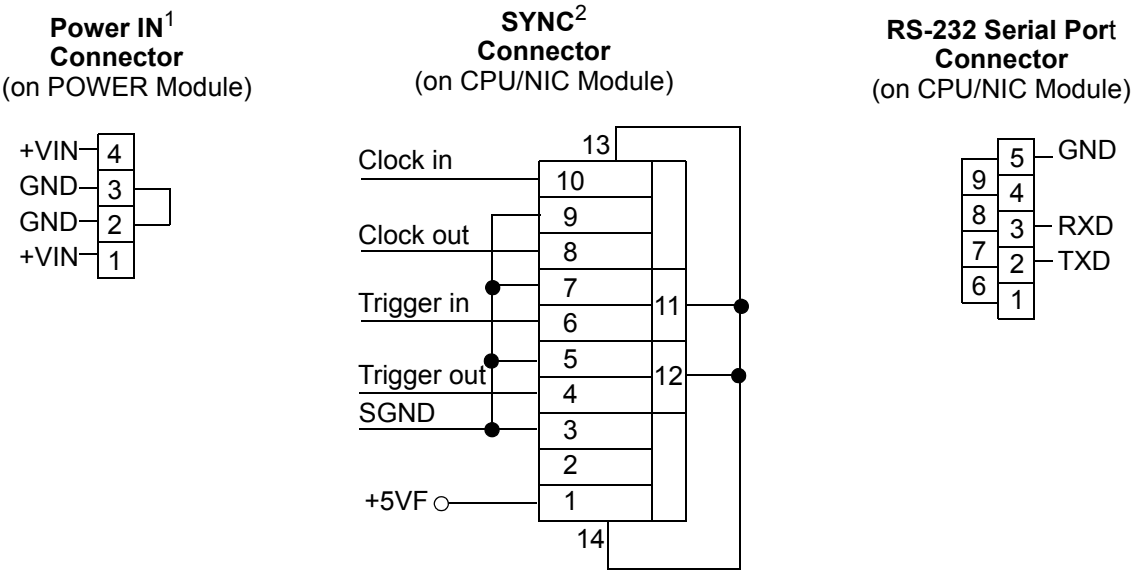
The operating conditions indicated by the front panel LEDs are described in the figures starting with Figure 1-9 on page 11 and ending with Figure 1-12 on page 13.

6.1.10 Watchdog Timer With Real-time Clock (Battery Backed)

The DNR-X-1G system includes a watchdog timer with battery backed-up real-time clock.

6.2.11 CPU / NIC Pinouts

Pinout diagrams for the various connectors on the DNR-CPU-1000 and DNR-POWER-DC Modules are shown in **Figure 6-3**.



[1]Mating connector available from DigiKey, Molex PN 39-01-4040

Figure 6-3. CPU / NIC Pinout Diagrams

Chapter 7 Programming Module-specific Functions

7.1 Overview

This chapter describes tools and facilities used for programming module-specific functions — memory maps for various CPUs, register descriptions, procedures for startup, setting parameters, loading/updating firmware, setting up triggers, synchronization, and clock lines.

The DNR-CPU-1000 Core Module has the following memory map:

Table 7-1. Memory Map

Device	Start Address	End Address	Size	Description
SDRAM	**0x0**	**0x8000000**	**128MB**	**SDRAM_ADDRESS**
Exception table	0x0	0x3000	12k	Processor address map
IMM	0x10000000			Memory map register - `IMM_ADDRESS`
On-board logic	0xA00E0000	0xA00EFFFC	64kB	EXT_SRAM_ADDRESS
Watchdog timer	0xA00E8000			`IOM_WDTIMER` – within PLD access space
Processor RAMBAR	0x80000000			
Module – CS2	0xA0000000	0xA00FFFFC	1MB	EXT_DEV_ADDRESS2
Module – CS3	0xA0100000	0xAFFFFFFC	256M	EXT_DEV_ADDRESS3
Flash (parameters)	0xFFC00000	0xFFC0FFFF	64kB	Parameters (64 sectors)
Flash (firmware)	0xFFC10000	0xFFEFFFFF	3MB	Firmare (3MB – 64kB)
Flash (U-Boot)	0xFFF00000	0xFFFFFFFF	1MB	U-Boot

Two address ranges are interesting for host software:

Module Address Space (0xA0000000 – 0xA00FFFFC and 0xA0100000 – 0xAFFFFFFC). The first address range is dedicated for devices located on the CS2 line and it accommodates sixteen modules with 64k memory map each. The second address range is designated for fast devices located in the CS3 line and it accommodates fifteen devices with 16MB memory map each.

7.2 Startup Sequence

After reset, the processor starts monitor execution from flash memory. The monitor initializes the processor and the address map, retrieves information from the parameter sector of the flash memory and tests system memory and other system resources.

If the "`fwgo`" parameter is set to "`autorun`", the monitor waits for three seconds for you to send Ctrl-A (which is transmitted over the serial interface.) If sent, the monitor aborts loading firmware into memory and brings up the monitor command prompt (to load new firmware, for example).

Otherwise, the monitor reads the firmware from the flash memory and stores it in RAM. Then, the monitor executes the firmware.

The following parameters are critical for firmware to be copied and started from the proper address:

```
fwad: 0xFFE40000
fwgo: 0x1
fwsz: 0x100000
fwcp: 0x20000
fwst: 0x20400
```

These parameters can be reviewed by using the "`show`" command while you are at the monitor "**#>**" prompt.

"**fwad**" is the initial address where firmware is stored. This address should be set before storing firmware or executing it.

"**fwgo**" defines whether the monitor should load firmware or display a command prompt.

"**fwsz**" defines the size of the stored firmware. Default value is 0x100000 – one megabyte.

"**fwcp**" defines the address to which the monitor copies firmware from flash memory. The default is 0x20000.The firmware is compiled to run from this address.

"**fwst**" defines the firmware entry point. The firmware entry point follows the vector table and is located with an offset 0x400 from the beginning of the firmware code.

These parameters are pre-programmed at the factory and there is no known reason for you to change them.

The monitor command "`fwjmp`" causes the monitor to load and execute firmware.

After reset, the processor reads the boot-up sequence located at 0xfffff100. This command sequence is a part of U-Boot code. U-Boot initializes all major subsystems of the CM including DDRAM and Ethernet interface.

After initializing, U-Boot performs a command list stored in its environment sector under the **bootcmd** entry. Standard commands to launch firmware are either **fwjmp** or **go** 0xffc10000, depending on the version of U-Boot installed. U-Boot then gives up control to the firmware code located at 0xffc10000. Firmware self-expands into the DDRAM, initializes the exception table, and starts execution.

7.3 Setting Core Module Parameters

There are two ways to set up Core Module (CM) parameters. The first one is the use of serial interface and the second one is the use of DaqBIOS calls.

To connect to the serial interface, you should connect a 9-wire serial extender cable to the DNR-12/6 CPU/NIC module (male plug connector) and your PC COM1 serial port (female connector). Some cables have female-to-female connectors, so you may have to use a gender-changer.

Set up your terminal to the proper serial port, 57600 bit rate, no parity, eight data bits, and one stop bit.

Alternately, using *Start→Run…*on the Microsoft Windows desktop, type *\Program Files\UEI\PowerDNA\Firmware\mttty.exe* Then click *File>>Connect*.

Once a connection to the PowerDNR DNR-X-1G system is established, tap "Enter" once. The DNR-X-1G should respond with either a "DQ>" prompt (this is firmware prompt) or a "**#>**" prompt (monitor prompt).

Once you see the "DQ>" prompt, you can type "**help<enter>**" to receive the list of all available commands.

The following commands are available:

```
DQ> help

    help Display this help message      help
     set Set parameter                  set option value
    show Show parameters                show
   store Store parameters (flash)       store
      mw Write wr <addr> <val> (hex)    mw
      mr Read rd <addr> (hex)           mr
    time Show/Set time                  time [mm/dd/yyyy] [hh:mm:ss]
    pswd Set password                   pswd {user|su}
      ps Show process state #           ps [value]
    test Test something                 test [test number]
   simod System Init/Module Cal         simod [routine]
   reset Reset system                   reset [all]
  dqping Send DQ_ECHO to <mac addr>     dqping [MAC|IP]
    mode Set current mode                mode
{init|config|oper|shutdown} [ID]
     log Display log content            log [start [end]] -1 = clear
     ver Show firmware version          ver
  devtbl Show all devices/modules       devtbl
 netstat Show network statistics        netstat
```

One of the most useful commands is "**show**":

```
DQ> show

        name: "IOM_22811"
       model: 0x1005
      serial: 0022811
         mac: 00:0C:94:00:59:1B
        fwct: 1.2.0.0
         srv: 192.168.0.229
          ip: 192.168.0.67
     gateway: 192.168.0.1
     netmask: 255.255.255.0
         udp: 6334
```

This command displays current values of every major DNR-X-1G parameter.

To change parameters, use the "**set**" command (type **set** for "**set**" command syntax).

```
DQ> set

Valid 'set' options:
```

```
        name: <Device name>
       model: <Model id>
      serial: <Serial #>
         mac: <my ethernet address>
        fwct: <autorun.runtype.portnum.umports>
         srv: <Host IP address>
          ip: <IOM IP address>
     gateway: <gateway IP address>
     netmask: <netmask IP address>
         udp: <udp port (dec)>
```

For example, to set a new IP address, type:

```
DQ> set ip 192.168.100.100
```

Other parameters can be changed the same way. Once parameters are set, however, you have to store them into non-volatile flash memory:

```
DQ> store
Flash: 1212 bytes of 1212 stored! CRC=0x8975E34A Old=0x8975E34A
Configuration stored
DQ>
```

After parameters are stored, you should reset firmware (start firmware execution from the beginning without full hardware reset), as follows:

```
DQ> reset
Stopping…

DaqBIOS (C) UEI, 2001-2004. Running PowerDNA Firmware
Built on 16:39:15 Oct  1 2004
Initialize uC/OS-II (Real-Time Kernel v.252)
Configuration recalled
3 device detected

Address    Irq  Model Option  Phy/Virt  S/N     Pri  DevN
-----------------------------------------------------------
0xA0000000   2    205    1    phys   0023115      10  0
0xA0010000   2    205    1    phys   0023117      20  1
0xA0020000   2    205    1    phys   0023119      30  2
-----------------------------------------------------------
Current time: 18:53:45 11/01/2004
IOM: TCP/IP/DQ stack. MAC=00:0C:94:00:59:1B
```

To perform a full hardware reset, use:

```
DQ> reset all
```

The full reset performs a physical reset of the CPU and initiates the whole startup sequence.

Some commands (such as `mr, mw, set,` and `store`) require entering a user password. Once the password is entered, these commands become enabled until firmware reset. There are two levels of password protection available. The first is user level and the second is super-user level. Super-user level is currently used only for updating firmware over the Ethernet link.

`DQ> pswd user` sets up a user level password. First, you'll be asked about your old password and then (if it matches) to enter the new password twice.

`DQ> pswd su` sets up super-user level password. First, you'll be asked about old super-user password and then (if it matches) to enter the new super-user password twice.

DNR-12 and DNR-6 systems come with the default password set to "`powerdna`".

Some DaqBIOS commands require clearing up user or super-user password. Use **DqCmdSetPassword()** before calling these functions. The PowerDNA API Reference Manual notes which functions are password-protected.

Another useful command is "`devtbl`". This command displays all I/O modules found and initialized by firmware along with assigned device numbers.

Use these device numbers in host software to address these devices.

Priority determines the order in which device drivers are located in the device stack. A device with a lower priority number receives a shared interrupt first. The firmware sets up device driver priorities when it registers device drivers.

"`simod`" is a command for system initialization and module calibration.

"`simod 0`" is used to initialize initial module parameters – serial number, option, etc. We do not recommend use of this command in the field.

"`simod 1`" allows module calibration. Different modules have different calibration procedures, explained in respective sections of this document.

"`simod 3`" allows you to perform factory tests – this is a non-destructive command.

WARNING: Once you use the "simod 0" command, the module warranty is void.

7.3.1 Setting Parameters Via Serial Interface

Using the serial interface, you can set up the following parameters:

```
    name: <Device name>
   model: <Model id>
  serial: <Serial #>
     mac: <my ethernet address>
    fwct: <autorun.runtype.portnum.umports>
     srv: <Host IP address>
      ip: <IOM IP address>
 gateway: <gateway IP address>
 netmask: <network mask>
```

```
udp: <udp port>
```

"**Name**" sets the device name (up to 32 characters)

"**Model**" sets the device model (factory programmed, do not change). A valid value is 0x3012.

"**Serial**" sets the DNR-12/6 serial number (factory programmed, do not change)

"**MAC**" sets the DNR-12/6 MAC Ethernet address (factory programmed, do not change)

"**fwct**" defines the behavior of the monitor upon boot-up. Valid values for "**autorun**" are zero – stay in monitor after initial boot sequence, or one – copy firmware to SDRAM memory location and execute from there.

"**runtype**" for the DNR-12/6 should be 2.

:**portnum**" and "**umports**" should be zero.

"**Srv**" sets the host IP address. You have to set the host IP address only if raw Ethernet protocol is in use (used in homogenous IOM networks only.) This parameter is ignored when the DNR-12/6 system is used over the UDP protocol or from the host.

"**IP**" specifies the IOM IP address. This is the most important parameter the user must change to allow the DNR-12/6 system to be visible on the network. The DNR-12/6 responds to every UDP packet containing a DaqBIOS prolog sent to this address. Since the current release does not support DHCP, the user should set up the IP address.

"**gateway**" specifies where the DNR-12/6 should send an IP packet if a requested IP packet exists outside of the DNR-1/62 network (defined by the network mask). Ask your system administrator if you use your DNR-12/6 on the office network.

"**netmask**" specifies what type of subnet the DNR-12/6 is connected to. The factory sets netmask to Type C IP network – 254 nodes maximum

"**udp**" specifies what port the firmware should use if a network packet originated from this DNR-12/6 without a previous request from the host side. If the DNR-12/6 replies to a DaqBIOS packet, it uses the source IP address from the IP packet header and source UDP port from UDP packet header.

Let's assume that you want to connect a DNR-12/6 to the dedicated network (secondary NIC adapter in the host PC).

Let's also assume that host IP address on this dedicated network is:

```
IP address: 192.168.100.28
Network mask: 255.255.255.0
Gateway: ignored
```

```
DNS: ignored
```

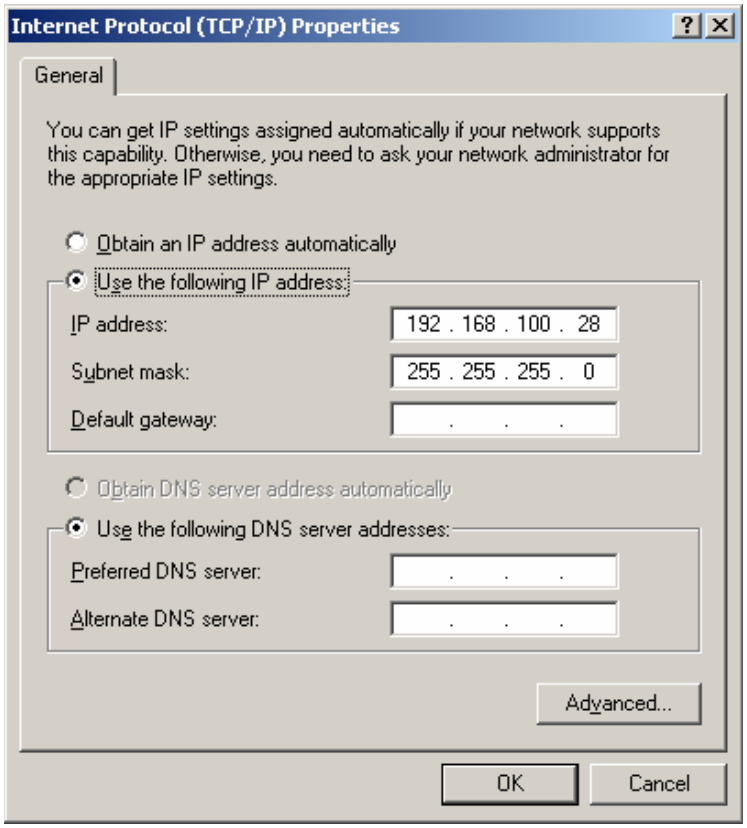

Internet Protocol (TCP/IP) Properties
General
You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings.
Obtain an IP address automatically
Use the following IP address:
IP address:
192 . 168 . 100 . 28
Subnet mask:
255 . 255 . 255 . 0
Default gateway:
Obtain DNS server address automatically
Use the following DNS server addresses:
Preferred DNS server:
Alternate DNS server:
Advanced...
OK
Cancel

Figure 7-1. TCP/IP Properties

Set DNR-12/6 system address to any address in the range of 192.168.100.1 through 192.168.0.254 excluding 192.168.100.28 – the host IP address.

For example, type:

```
DQ> set ip 192.168.0.2
```

Then:

```
DQ> store
```

This sequence of commands stores a new IP address in the flash parameter sector. Then, you have to reset the DNR-12/6 system.

DNR-12/6 systems come from the factory with IP addresses already preset for 192.168.x.x network. The factory IP address can be found on the label located on the back of the DNR-12/6 enclosure along with factory-set MAC address.

After the IP address is set, you can establish communication with the DNR-12/6 system using PowerDNA Explorer.

7.3.2 Clock and Watchdog Access

To show and set up the date and time, use the "**time**" command, as follows:

```
DQ> time
Current time: 17:39:22 11/01/2004
```

To set up time of the day, enter:

```
DQ> time 17:40:00
```

To set up date, enter:

```
DQ> time 11/03/2004
```

Date and time are stored in the battery-backed real-time clock chip.

7.4 Common Module (Layer) Interface

The Common Layer Interface is the protocol used in a PowerDNR system for communication between the IOM and its layers (I/O boards).

7.4.1 Channel List

A channel list specifies what channels and in which sequence each should be acquired/output. Every module has its own specific set of channel list flags. The firmware takes care of this hardware dependency. Please refer to the specific module description to find out what channel list flags are supported.

Users should use the following flags, generalized for all modules.

```
// Channel list entries definition - lower 16 bits are reserved for
                            // channel number
                           // gain and special, module-specific settings
#define DQ_LNCL_NEXT    (1UL<<31)    // channel list has next entry
#define DQ_LNCL_INOUT   (1UL<<30)    // input or output subsystem
#define DQ_LNCL_SS1     (1UL<<29)    // subsystem (high)
#define DQ_LNCL_SS0     (1UL<<28)    // subsystem (low)
#define DQ_LNCL_IRQ     (1UL<<27)    // fire IRQ
#define DQ_LNCL_NOWAIT  (1UL<<26)    // execute this step but don't
                                      // wait
                                     // for the next CV
#define DQ_LNCL_SKIP    (1UL<<25)    // execute this step and discard
                                        // data
                                     // for the next CV
#define DQ_LNCL_CLK     (1UL<<24)    // wait for the next channel list
                                        //  clock
#define DQ_LNCL_CTR     (1UL<<23)    // clock counter once
#define DQ_LNCL_WRITE   (1UL<<22)    // write to the channel but do
                                      // not update
#define DQ_LNCL_UPDALL  (1UL<<21)    // update all written channels
#define DQ_LNCL_TSRQ    (1UL<<20)    // copy TS along with data (i+=2)
#define DQ_LNCL_SLOW    (1UL<<19)    // slow down operation
#define DQ_LNCL_RSVD2   (1UL<<18)    // reserved
#define DQ_LNCL_RSVD1   (1UL<<17)    // reserved
#define DQ_LNCL_RSVD0   (1UL<<16)    // reserved
#define DQ_LNCL_DIFF    (1UL<<15)    // differential mode
```

There are a few helper macros defined to simplify setting gain and subsystem flags, as follows:

```
#define DQ_LNCL_GAIN(G) ((G & 0xf)<<8)   // set gain
#define DQ_LNCL_GETGAIN(E)  ((E & 0xf00)>>8)  // pull out gain
#define DQ_LNCL_GETCHAN(E)  (E & 0xff)        // pull out channel
#define DQ_EXTRACT_SS(flags) (((flags) & (LNCL_SS1 | LNCL_SS0)) >>28)
#define DQ_EXTRACT_DIR(flags) (((flags) & LNCL_INOUT) >> 30)
#define DQ_SS_DIR(ss, dir) (((ss) << 1) | (dir))
```

The configuration flags serve different functions:

`DQ_LNCL_NEXT` – specifies that there is a following channel list entry in the channel list. A channel list entry without this flag set is considered the last one. Advanced and ACB functions add this flag automatically

`DQ_LNCL_INOUT` – specifies whether this is an input or output channel for multifunction modules

`DQ_LNCL_SS1` – specifies the subsystem to which the channel belongs. Do not use for single-subsystem modules

`DQ_LNCL_SS0` – specifies the subsystem to which the channel belongs. Do not use for single-subsystem modules

`DQ_LNCL_IRQ` – causes the module to fire an IRQ upon processing this entry. Required for special real-time cases

`DQ_LNCL_NOWAIT` – causes the module to temporarily “forget” about the CV clock and start execution of the next channel list entry right after the current one is completed

`DQ_LNCL_SKIP` – prohibits storing the data specified in this channel list entry into the data output FIFO or prohibits advancing the data input FIFO pointer. This flag is used to increase the settling time

`DQ_LNCL_CLK` – causes the channel list machine to wait for the next channel list clock. Normally, the state machine executes the whole channel list on a single CL clock.

`DQ_LNCL_CTR` – perform a pulse on the selected line. This flag is used for synchronization purposes

`DQ_LNCL_WRITE` – write the output to the double-register but do not propagate the physical signal to the output.

`DQ_LNCL_UPDALL` – clock all output channel double-registers to update them simultaneously. This entry is usually used with the `DQ_LNCL_WRITE` entry when you need to write data to the output channels sequentially and update them at the same time. In this situation, you should use the `DQ_LNCL_WRITE` flag for every entry. To update all outputs with previously written values, combine the `DQ_LNCL_WRITE` flag with the `DQ_LNCL_UPDALL` flag.

`DQ_LNCL_TSRQ` – insert a timestamp into the output data

`DQ_LNCL_SLOW` – double the settling time for this channel

`DQ_LNCL_DIFF` – acquire the channel in differential mode (rather than single-ended or pseudo-differential)

The channel number occupies the first eight bits of the channel list entry. The maximum number of channels on one device cannot be larger than 256.

Bits [11…8] contain gain information. The number of gains and the gain are specific for every module type. See powerdna.h for module-specific gain macros.

7.4.2 Configuration Flags

Configuration flags occupy a 32-bit configuration word. The upper part of the configuration word contains module-specific flags.

```
// Standard part (lower 16 bits) of module configuration word
// Please notice that for multiple-subsystem modules you should pass
// multiple configuration uint32s in config_io()
//
#define DQ_LN_TSCOPY     (1L<<18)  // copy timestamp along with the
                                   // data
#define DQ_LN_MAPPED     (1L<<15)  // For WRRD (DMAP) devices
#define DQ_LN_STREAMING  (1L<<14)  // For RDFIFO devices - stream the
                                    //FIFO data automatically
                                 // For WRFIFO - do NOT send reply
                                   // to WRFIFO unless needed
#define DQ_LN_RECYCLE    (1L<<13)  // if there is no data taken
                                    // available
                                   // overwrite/reuse data
#define DQ_LN_GETRAW     (1L<<12)  // force module to return raw
                                  // unconverted
                                   // data
#define DQ_LN_TMREN      (1L<<11)  // enable module periodic timer
#define DQ_LN_IRQEN      (1L<<10)  // enable module irqs
#define DQ_LN_PTRIGEDGE1 (1L<<9)   // stop trigger edge MSB
#define DQ_LN_PTRIGEDGE0 (1L<<8)   // stop trigger edge: 00-software,
                                   // 01- rising,
                                   // 02 - falling
#define DQ_LN_STRIGEDGE1 (1L<<7)   // start trigger edge MSB
#define DQ_LN_STRIGEDGE0 (1L<<6)   // start trigger edge: 00-software,
                                   // 01 - rising, 02 - falling
#define DQ_LN_CVCKSRC1   (1L<<5)   // CV clock source MSB
#define DQ_LN_CVCKSRC0   (1L<<4)   // CV clock source 01 - SW,
                                 // 10 - HW, 11 - EXT
#define DQ_LN_CLCKSRC1   (1L<<3)   // CL clock source MSB
#define DQ_LN_CLCKSRC0   (1L<<2)   // CL clock source 01 - SW,
                                   // 10 - HW, 11 - EXT
#define DQ_LN_ACTIVE     (1L<<1)   // "STS" LED status
#define DQ_LN_ENABLED    (1L<<0)   // enable operations
```

`DQ_LN_ACTIVE` is needed to switch on the "STS" LED on CPU module.

`DQ_LN_ENABLE` enables all operations within the module

`DQ_LN_CLCKSRC0` selects the internal channel list clock (CL) source as a time base. AI-201 supports the CL clock only where the time between consecutive channel readings is calculated by the rule of maximizing setup time per channel. If you'd like to clock CL, clock from an external clock source such as SYNCx line, set the `DQ_LN_CLCKSRC1` flag as well.

DQ_LN_CVCKSRC0 selects the internal conversion clock (CV) source as a time base. Setting CV clock allows having an equal time period between conversions of different channels. It is mostly used when you are interested in a phase shift between channels.

You can select either the CL or CV clock as a time base. If both clocks are selected, the CL clock is taken as a time base and the CV clock determines the delay between converting channels (i.e. setting time.)

IS

DQ_LN_STRIGEDGE0, DQ_LN_STRIGEDGE1 define the start trigger edge and source. The source can be either software command or external trigger edge.

DQ_LN_PTRIGEDGE0, DQ_LN_PTRIGEDGE1 define the stop trigger edge and source. The source can be either software command or external trigger edge.

DQ_LN_TSCOPY – copy timestamp at the end of every channel list

DQ_LN_MAPPED - set this flag to declare DMap mode

DQ_LN_STREAMING - set this flag to declare ACB mode

DQ_LN_RECYCLE - this flag affects output operation. If this flag is set and module does not receive output data, it will recycle old data until new data is available; otherwise, the module will stop at the last value output

DQ_LN_GETRAW - tells the module to return uncalibrated unconverted data. This flag makes sense only for modules with software calibration (AI-225, for example). Moving calibration and conversion of data to host unloads the IOM processor

DQ_LN_TMREN - use a real-time timer to retrieve data from the PowerDNA cube. When this mode is selected, the firmware programs the module to store one channel list worth of data in the buffer. On a timer tick, the firmware transfers this data from the module output buffer to the packet. This function is used when the hardware allows only a selected set of update rates, but you need something in between. For example, AI-225 can convert data with fixed frequency equal 6.875Hz * 2^n, where n = [0…9]. To receive an exactly 500Hz data stream from this module, specify that this module be updated upon a timer tick.

DQ_LN_IRQEN - use interrupts to retrieve data from the module output buffer via packets. This is preferable mode of operation.

7.4.3 EEPROM User Area Access

Every I/O module has an E^2PROM chip that contains 2048 bytes of module-specific information.

Model and option numbers identify every module. The model number is hard-coded inside module logic and option numbers are stored inside E^2PROM.

E^2PROM is divided into certain access areas (some of them can be missing in different module types):

```
typedef struct {
    DQEECMNDEVS ee;
    DQCALSET_xxx_ calset;
    DQOPMODEPRM_xxx_ opmodeprm;
    DQINITPRM_xxx_ initprm;
    DQSDOWNPRM_xxx_ sdownprm;
    DQCNAMES_xxx_ cname;
} DEVEEPROM_xxx_, *pDEVEEPROM_xxx_;
```

The first part of the module E^{2}PROM is common device information defined as:

```
typedef struct {
    /* header is standard for all devices */
                        /* superuser access */
    uint16  model;      /* device model to verify EEPROM identity */
    uint16  option;     /* device option */
    uint16  total;   /* total EEPROM size - EEPROM read is expensive*/
                   /* if this field <32 or >2048 read all2048 bytes */
    uint32  sernum;     /* serial number - pad to %07d when printing */
    uint32  mfgdate;    /* manufacturing date:  0xmmddyyyy */
                        /* user access */
    uint32  caldate;    /* calibration date:    0xmmddyyyy */
    uint32  calexpd;    /* calibration expired: 0xmmddyyyy */

    /* header is followed by device-specific data structures */
} DQEECMNDEVS, *pDQEECMNDEVS;
```

`CALSET_xxx_` contains module calibration information. Firmware writes this information automatically upon entering initialization mode.

`OPMODEPRM_xxx_` contains module parameters for operation mode. For example, AI-201 has the following parameters stored:

```
typedef struct {
    uint32 chlst[AI201_CHAN];   // channel list - full
    uint32 conf;                // control word - module API flags
    uint32 cvclk;               // CV clock
    uint32 clclk;               // CL clock
    uint32 trig;                // trigger configuration
…
} DQOPMODEPRM_201_, *pDQOPMODEPRM_201_;
```

This structure varies from one major firmware revision to another.

When the firmware switches the module into operation mode, it processes stored configuration information as it would process configuration parameters received from host. All working fields in the internal device information structure are filled and the unit is ready to switch into operation mode. By programming the `DQOPMODEPRM` structure ahead of time and storing it into E^{2}PROM, you can avoid programming the IOM every time before switching into operation mode.

`INITPRM_xxx_` contains initial I/O directions and output levels. The firmware sets up the direction and the level on every output line on entering initialization state.

`SDOWNPRM_xxx_` contains final I/O directions and output levels. The firmware sets up the direction and the level on every output line on entering shutdown state.

`CNAMES_xxx_` contains channel names. The length of the channel names depends on the module type. Only 512 bytes are allocated for channel names. Thus, AI-205 module (four channels) can have channel names as long as 32 characters while DIO-403 channel names (48 channels) cannot be longer then 10 characters.

There is a set of functions written to read, write, and store these parameters into E^2PROM. Functions `DqCmdGetParameters()`/`DqCmdSetParameters()` access modal parameters, while `DqCmdSaveParameters()` stores parameters into E^2PROM.

7.4.4 PowerDNA Module Signaling

This section defines procedures for setting up triggering, synchronization, and clocking lines.

Most PowerDNA modules have the following interconnection diagram:

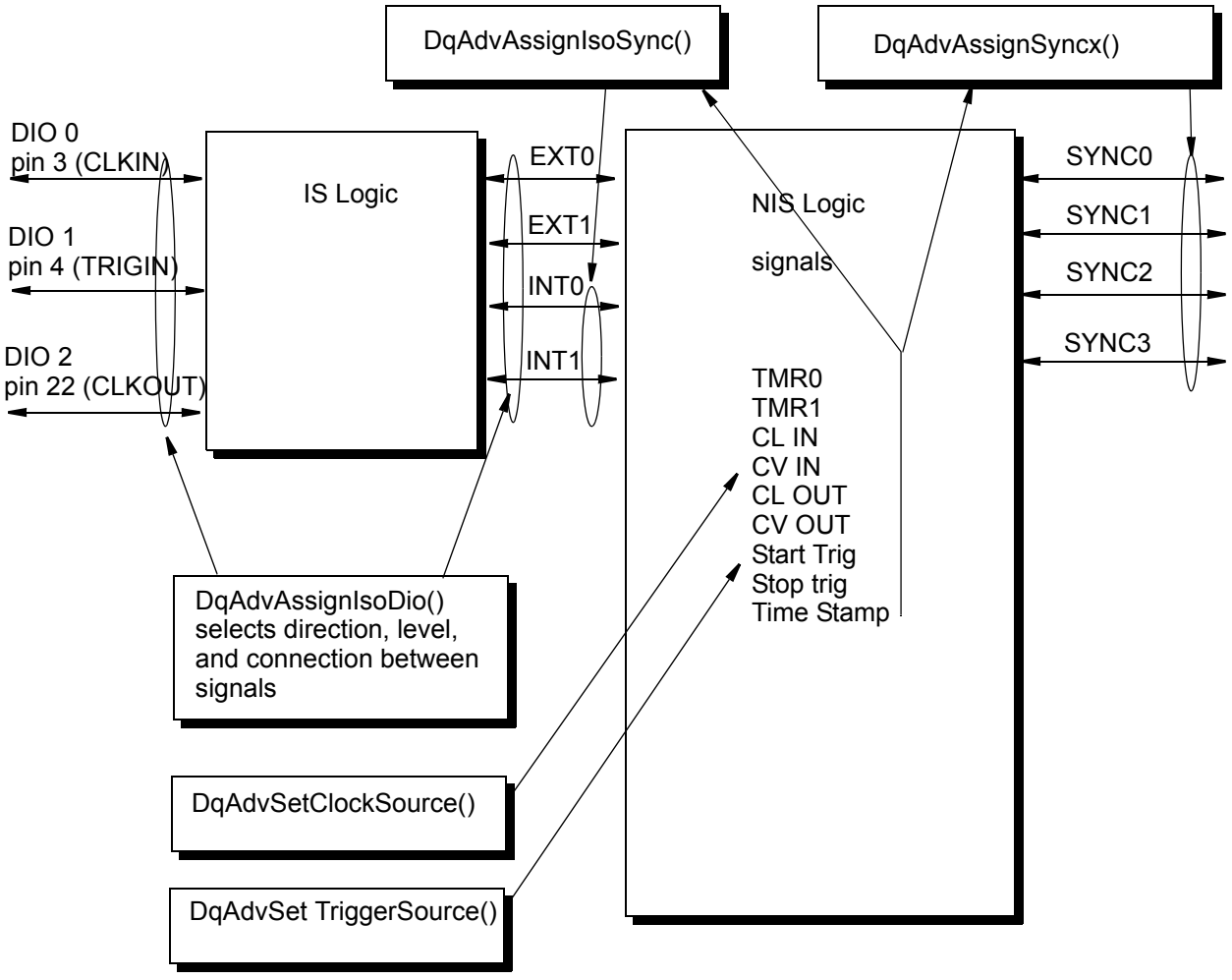


Figure 7-2. Core Module Interconnection Diagram

- DIO0/CLKIN – pin 3 on the FJIO1 DB-37 connector. By default, this pin is an input, connected to the ISO_EXT0 synchronization line and through this line to the NIS logic

- DIO1/TRIGIN – pin 4 on the FJIO1 DB-37 connector. By default, this pin is an input, connected to the ISO_EXT1 synchronization line and through this line to the NIS logic
- DIO2/CLKOUT – pin 22 on the FJIO1 DB-37 connector. By default, this pin is an output connected to the ISO_INT0 line from the NIS logic

The PowerDNA API exposes six specially designated functions to control these lines, as follows:

- `DqAdvSetClockSource()`

  This function selects external clock source for CL (or CV) clock. Clock can be selected from internal sources, EXTx lines (signals from the isolated side) and SYNCx interface signals (inputs)

- `DqAdvSetTriggerSource()`

  This function selects external clock source for start and stop trigger. Clock can be selected from internal sources, EXTx lines (signals from the isolated side) and SYNCx interface signals (inputs)

- `DqAdvAssignIsoDio()`

  This function selects direction and signal assignment for external DIO line. EXT0/1 lines are assigned to DIO0/1 lines when DIO lines are in the input state.

- `DqAdvAssignIsoSync()`

  This function selects signal assignment for INT lines. This function allows selecting what signal from isolated side of the module logic will be assigned to INTx lines. Signals can be selected from internal clock sources and SYNCx lines.

- `DqAdvAssignSyncx()`

  This function selects a signal for each of the SYNCx lines. When a SYNC line is selected, it switches to the output state. All other modules “listen” to this command on the system bus and release that SYNC line from use (switch to the input mode). This organization prevents two modules from driving the same line.

- `DqAdvWriteSignalRouting()`

  This function writes and activates selected signal routing. This function transfers created configuration to the cube and activates it. Cube sends current synchronization configuration as a reply.

NOTE: Note that to take advantage of using external clocks for the module clock and/or trigger, the source should be selected as external. This means that, in clocking configurations, the following bits should be set up:

```
DQ_LN_CLCKSRC1 – external CL clock is selected
DQ_LN_STRIGEDGE1 – external start trigger is selected
DQ_LN_PTRIGEDGE1 – external stop trigger is selected
```

If internal sources are selected for those signals, all external signal configurations do not affect module clocking.

The same interface applies to the CPU module. The CPU module has one external input and one output routable to the SYNCx interface as well as multiple clocks. It is possible to include an IEEE 1588 implementation with an atomic clock (1us) resolution in the future.

NOTE

For a detailed description of the PowerDNx Protocol and the various Operating Modes for the Cube, including a discussion of Host / IOM Communication, Operation of the DAQBIOS Protocol, Real-Time Operation with an IOM, and Asynchronous operation with an IOM, refer to the document entitled PowerDNx Protocol and Operating Modes for PPCx, PPCx-1G, Cubes and DNR-x-1G HalfRACK and RACKtangle Chassis Document PN Man-DAQBIOS Protocol 1010, Version 1.0

Appendix A

A.1 Configuring a Second Ethernet Card Under Windows XP

To configure a second Ethernet card for your system, use the following procedure:

A. Set Up Your Ethernet Card (NIC).

If you already have an Ethernet card installed, skip ahead to the next section, “Configure TCP/IP”.

If you have just added an Ethernet card, to install it, do the following:

STEP 1: From the *Start* menu, select *Control Panel*, and click *Printers and Other Hardware*.

STEP 2: From the menu on the left, click *Add Hardware* and follow the on-screen instructions.

NOTE: We recommend that you allow Windows XP to search for and install your Ethernet card automatically. If Windows XP does not find your Ethernet card, you will need to install it manually by following the manufacturer's instructions.

Once your Ethernet card has been installed, continue to the next section.

B. Configure TCP/IP.

STEP 1: From the *Start* menu, select *Control Panel*.

STEP 2: Under the heading *Pick a Category*, click *Network and Internet Connections*.

STEP 3: Under pick a *Control Panel* icon, click *Network Connections*.

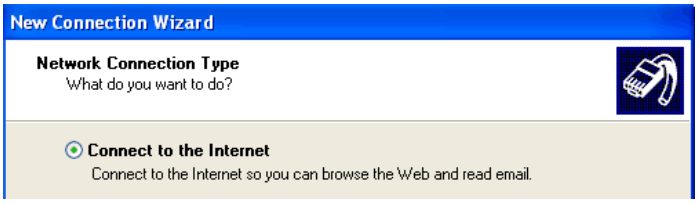
STEP 4: If you see an icon under *LAN* or *High-Speed Internet* heading for your second NIC, skip ahead to step 10.

STEP 5: If there is no icon under *LAN* or *High-Speed Internet* for your second NIC, proceed to step 4.

STEP 6: From the menu on the left, click *Create a new connection* to launch the *New Connection Wizard*.

STEP 7: Click *Next* and proceed to the *Network Connection Type* window.

STEP 8: Select *Connect to the Internet* and click *Next*.


New Connection Wizard
Network Connection Type
What do you want to do?
Connect to the Internet
Connect to the Internet so you can browse the Web and read email.

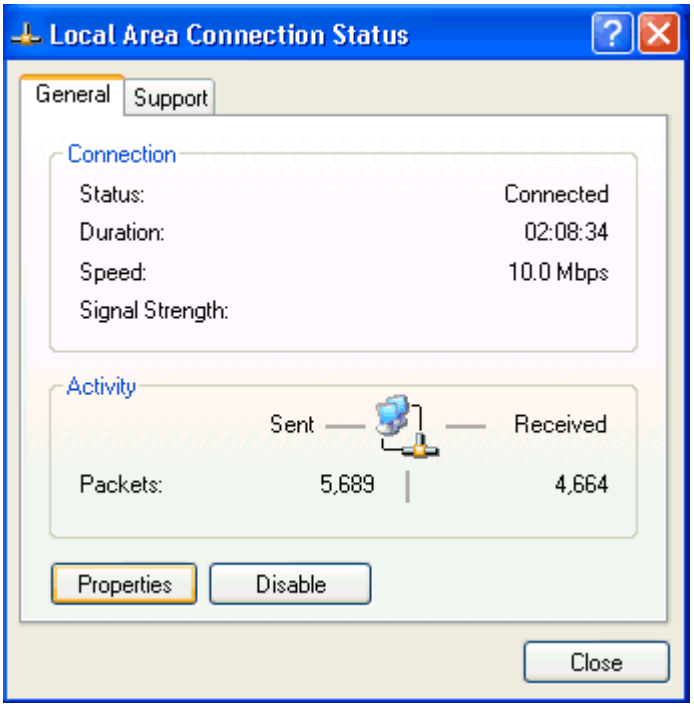
STEP 9: Select *Set Up My Connection Manually* and click *Next*.

STEP 10: Select *Connect Using a Broadband Connection that is always on* and click *Next*.

STEP 11: Click *Finish*.

STEP 12: In the *Network Connections* window, double-click the second icon under *LAN or High-Speed Internet.*

STEP 13: In the next window (see illustration below), click *Properties*.



STEP 14: Click the *General* tab, click once on *Internet Protocol (TCP/IP)*, then click *Properties*.

STEP 15: Click the *General* tab, click *Use the Following IP Addresses*, and in the corresponding boxes, enter `192.168.100.1` for the IP address, `255.255.255.0` for the Subnet Mask, and leave blank the router (or default gateway) information.

STEP 16: Click *Use the Following DNS Server Addresses*.

STEP 17: Make sure the *Preferred DNS Server* box and the *Alternate DNS Server* box are blank.

STEP 18: Click *OK* or *Close* until you return to the *Network Connections* window.

STEP 19: Close the *Network Connections* window.

B. Troubleshooting

If you encounter problems connecting to the network, first check to make sure the Windows XP Internet Connection Firewall is turned off. Follow the instructions below:

STEP 1: From the *Start* menu, select *Control Panel*.

STEP 2: Under the heading *Pick a Category*, click *Network and Internet Connections*.

STEP 3: Under pick a *Control Panel* icon, click *Network Connections*.

STEP 4: Double-click the icon under *LAN or High-Speed Internet*. In the next window, click *Properties*.

STEP 5: Click the *Advanced* tab and uncheck the box *Protect My Computer and Network* by limiting or preventing access to this computer from the Internet (see illustration below).

Local Area Connection Properties
General
Authentication
Advanced
Internet Connection Firewall
Protect my computer and network by limiting or preventing access to this computer from the Internet
Learn more about Internet Connection Firewall.

STEP 6: Click *OK* or *Close* until you return to the *Network Connections* window.

STEP 7: Close the *Network Connections* window.

C. Using the Windows XP Alternate Configuration Setting

If you're using a computer with only one Ethernet port, such as a laptop, you can configure Windows XP to automatically switch settings depending on which network it's connected.

Windows XP users have the ability to configure a second IP address setting under the Control Panel that will allow Windows to pick the correct computer IP setting, based on the device that it finds connected to the Ethernet port. Under this configuration, your primary IP setting is configured for *Obtain IP Address Automatically* for connection to your company Network, and your secondary IP setting (Alternate Configuration) is configured for 192.168.100.1 with a subnet mask of 255.255.255.0 for connection to the PowerDNA cube, or DNR-12/6.

The following steps allow you to configure your alternate IP address, starting at the Control Panel.

STEP 1: Double click on *Network Connections*

STEP 2: Double click on *Local Area Connections*

STEP 3: Click on the *Properties* button

STEP 4: Select *Internet Protocol (TCP/IP)* and click on the *Properties* button

STEP 5: Select the *Alternate Configuration* tab

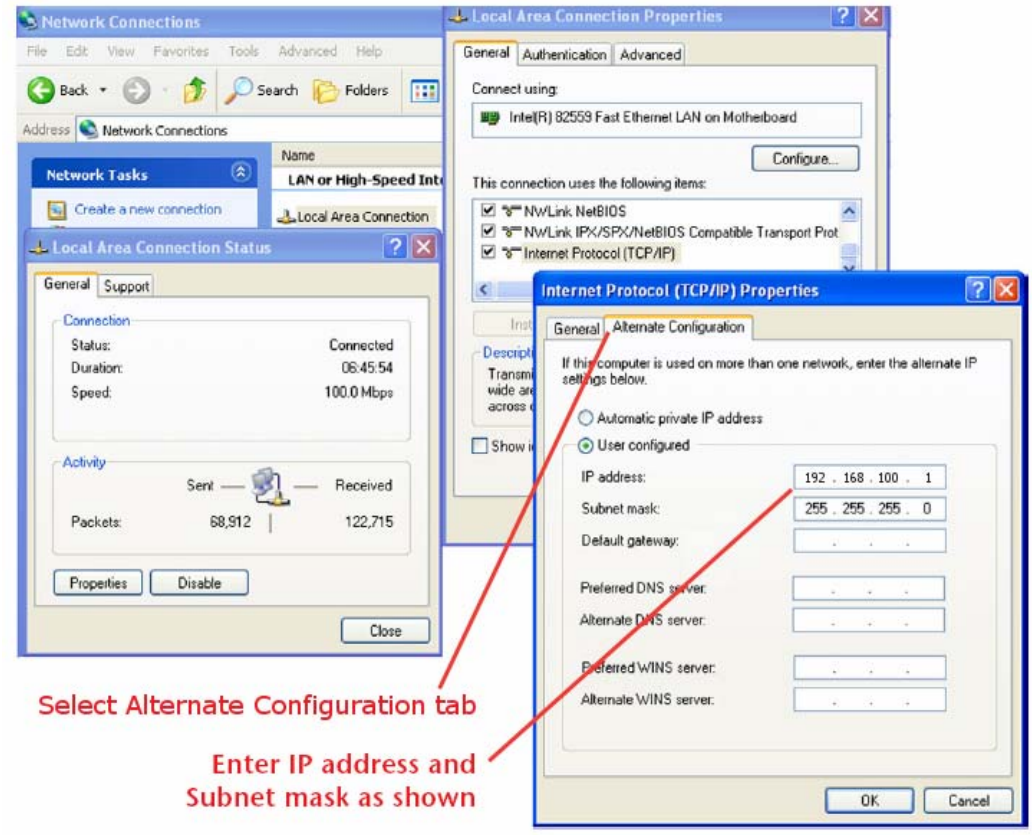
STEP 6: Select *User Configured*

STEP 7: Enter `192.168.100.1` for the *IP address*

STEP 8: Enter `255.255.255.0` for the *Subnet mask*

STEP 9: Close all open configuration windows using *OK* or *Close*

Use the following screen to configure the *Alternate Configuration* tab located under the Windows XP network configuration screen located in the Windows XP Control Panel.



Once you have this configuration in place, your computer will look for the attached device on your Ethernet port during “Boot Up” or during a Windows “Log On” operation. If it sees a powered on PowerDNA cube connected to the Ethernet port, it will automatically switch to using the secondary IP address. If the computer sees a DHCP network connected to the Ethernet port, it will use the primary IP configuration and negotiate an IP address with your company network as required.

If you are in the office and you want to check your email: Plug in the Ethernet cable for your company’s network connection into your computer and either power up your computer and log onto the network as you normally do, or if your computer is already powered on, perform a Windows “Log Off” and then a “Log On” and log onto your company network as you normally do.

If you are working in the field with a PowerDNA cube or DNR-12/6: Plug in the Ethernet cable from the data acquisition system into your computer and make sure that the data acquisition system is powered on. Then, either power up your computer and bypass your network log on screens, or if your computer is already powered on, perform a “Log Off” and then a “Log On” and bypass your network logon screens.

D. Configuring a Second Ethernet Card Under Windows 2000

This section describes procedures for configuring a second Ethernet Card under Windows 2000.

The procedure is as follows:

A. Set Up Your Ethernet Card (NIC)

Windows 2000 will normally detect and install your Ethernet card and TCP/IP automatically. To check that your card has been installed, run through the following steps.

STEP 1: From the *Start* menu, select *Settings* and then select *Network and Dial-up Connections*.

STEP 2: If you see a *Local Area Connection* icon, your Ethernet card has been detected and installed, skip ahead to the section *Configure TCP/IP*. If you do not see this icon, proceed to step 3.

STEP 3: From the *Start* button, select *Settings*, then *Control Panel*. Double-click on the *Add/Remove Hardware* icon and follow the on-screen instructions. We recommend that you allow Windows 2000 to search for and install your Ethernet card automatically. If Windows 2000 does not find your Ethernet card, you will need to install it manually by following the manufacturer's instructions.

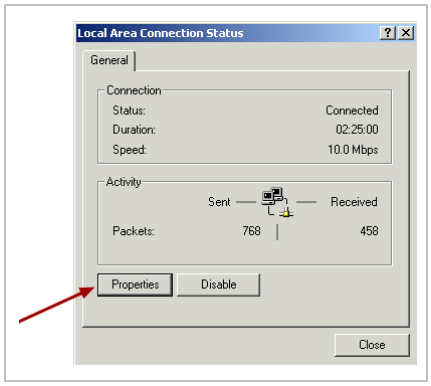
STEP 4: Once your Ethernet card has been installed, click *OK* and continue with the next section.

B. Installing TCP/IP

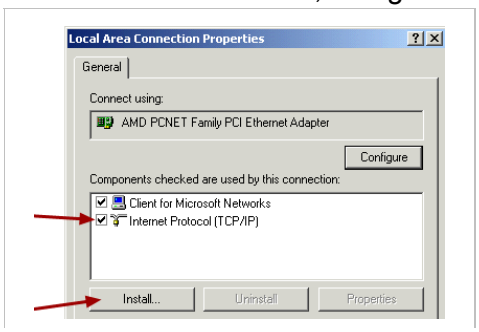
STEP 1: From the Start menu, select Settings and then select Network and Dial-up Connections.

STEP 2: In the Network and Dial-up Connections window, double-click on the Local Area Connection 2 icon

STEP 3: In the Local Area Connection 2 Status window, click Properties:.

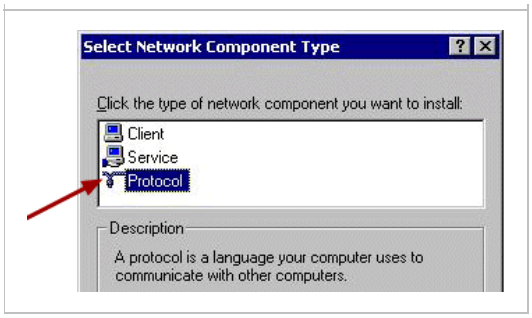


STEP 4: If Internet Protocol (TCP/IP) is listed, make sure the box next to it contains a check mark, and go to Configure TCP/IP..

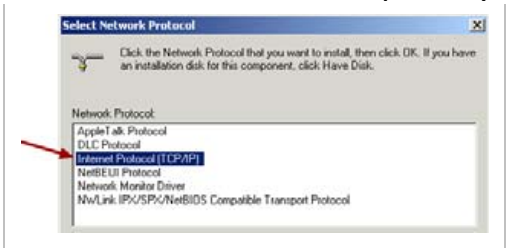


STEP 5: If Internet Protocol (TCP/IP) is not listed, click on Install.

STEP 6: In the next window, double click on Protocol..


Select Network Component Type
Click the type of network component you want to install:
Client
Service
Protocol
Description
A protocol is a language your computer uses to communicate with other computers.

STEP 7: ***Select Internet Protocol (TCP/IP), and click OK***.


Select Network Protocol
Click the Network Protocol that you want to install, then click OK. If you have an installation disk for this component, click Have Disk.
Network Protocol:
AppleTalk Protocol
DLC Protocol
Internet Protocol (TCP/IP)
NetBEUI Protocol
Network Monitor Driver
NWLink IPX/SPX/NetBIOS Compatible Transport Protocol

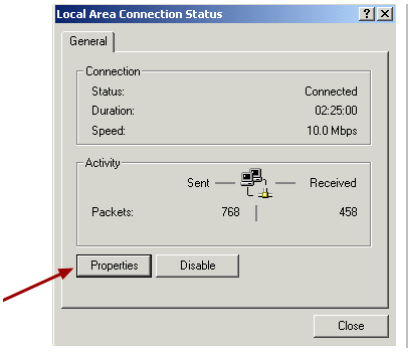
STEP 8: Make sure the box beside *Internet Protocol (TCP/IP)* contains a check mark, and proceed to the next section, *Configure TCP/IP*.

C. Configure TCP/IP

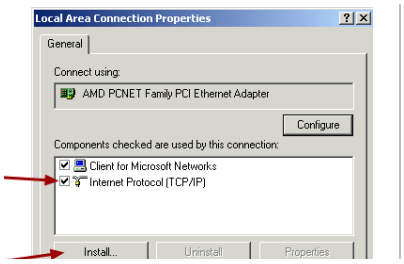
STEP 1: From the Start menu, select Settings and then select Network and Dial-up Connections.

STEP 2: In the Network and Dial-up Connections window, double-click on the Local Area Connection 2 icon.

STEP 3: In the Local Area Connection 2 Status window, click Properties:



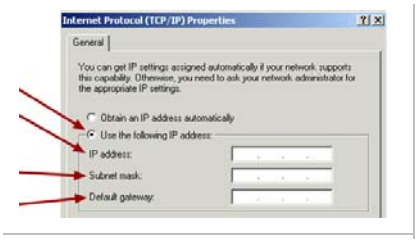
STEP 4: Click once on Internet Protocol (TCP/IP). Then click Properties.



STEP 5: Select *Use the following IP address*, and type `192.168.100.1`

In the Subnet mask box, type `255.255.255.0`.

Leave the Default Gateway box blank.



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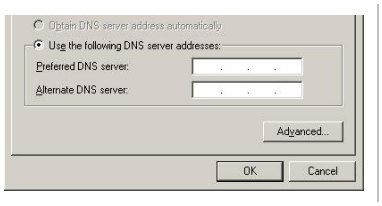
STEP 6: 6Select *Use the following DNS server addresses* and:
Make sure the *Preferred DNS server* box and the *Alternate DNS server* boxes are blank.



STEP 7: Click *OK*, click *OK* in the *TCP/IP Properties* window, click *OK* in the *Local Area Connection* window and click *Close* in the *Local Area Status* window.

STEP 8: Close the *Network and Dial-up Connections* window.

E. Configuring a Second Ethernet Card Under Windows NT

Set Up Your Ethernet Card (NIC)

If you installed your Ethernet interface before (or at the same time as) you installed Windows NT, then the system should have automatically detected it and you should proceed to the next section, “Install and Configure TCP/IP.” Optionally, you may follow steps 1-3 below to confirm that your interface is recognized.

If you obtained an Ethernet interface after Windows NT was already on your computer, do the following:

STEP 1: From the Start menu, select *Settings* and then select *Control Panel*.

STEP 2: Double-click on the *Network* icon.

STEP 3: Click on the tab labeled Adapters. You should then see an entry for your Ethernet card. If you do not see one, continue to step 4 to install it. Otherwise, click OK and skip ahead to Install and Configure TCP/IP.

STEP 4: Click Add... and follow the on-screen instructions. Select your Ethernet card from the list shown, or, if it is not included in the list, click Have Disk... and insert the diskette that came with the card. Even if your card does appear in the list, it's a good idea to use the diskette to make sure you have the latest drivers.

STEP 5: Restart your computer if Windows gives you the option to do so. Wait for the system to restart before continuing with the next section.

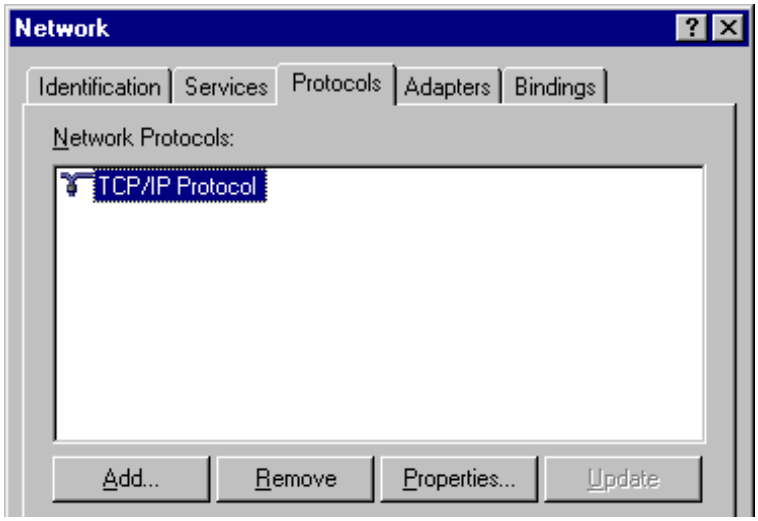
B. Install and Configure TCP/IP

STEP 1: From the Start menu, select Settings and then Control Panel.

STEP 2: Double-click on the Network icon, then click the Protocols tab.

STEP 3: In the list of Network Protocols, look for TCP/IP Protocol. If you don't see it, click Add..., select TCP/IP Protocol, and then click OK.

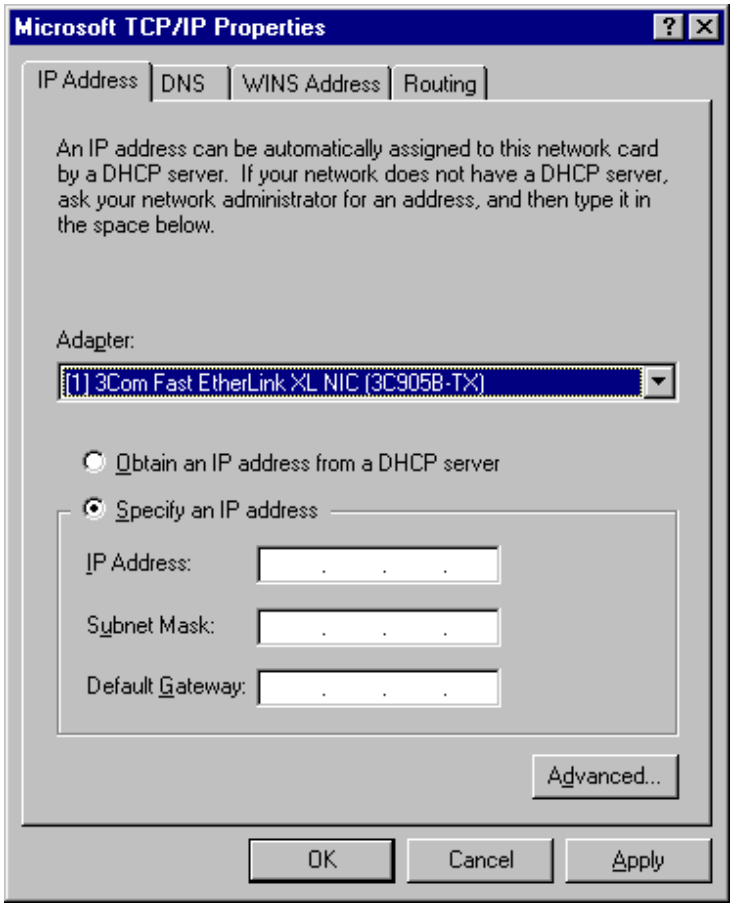
STEP 4: Select TCP/IP Protocol in the list of Network Protocols and then click Properties... A Microsoft TCP/IP Properties window will open.



STEP 5: Click on the IP Address tab if it is not already selected.

STEP 6: Make sure that the radio button next to Specify an IP address is selected.

STEP 7: Enter `192.168.100.1` for IP Address, `255.255.255.0` for Subnet Mask, and leave blank the Gateway Address (in the Default Gateway box.)


Microsoft TCP/IP Properties
IP Address
DNS
WINS Address
Routing
An IP address can be automatically assigned to this network card by a DHCP server. If your network does not have a DHCP server, ask your network administrator for an address, and then type it in the space below.
Adapter:
[1] 3Com Fast EtherLink XL NIC (3C905B-TX)
Obtain an IP address from a DHCP server
Specify an IP address
IP Address:
Subnet Mask:
Default Gateway:
Advanced...
OK
Cancel
Apply

STEP 8: Click on the DNS tab.

Leave blank the Host Name and Domain fields.

STEP 9: Click OK to close the Microsoft TCP/IP Properties window.

STEP 10: Click Close to close the Network control panel.

STEP 11: Restart your computer.

STEP 12: You should now be able to access network-based services.

F. Configuring a Second Ethernet Card Under Windows 95/98/SE/ME

Set Up Your Ethernet Card (NIC)

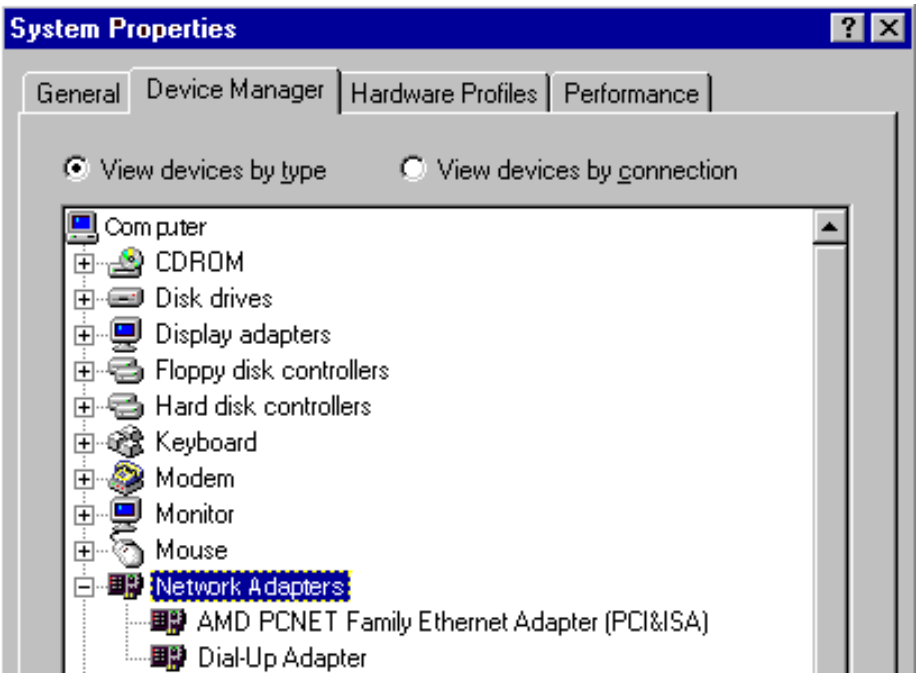
If you installed your Ethernet card before (or at the same time as) you installed Windows 95/98/ME, then the system should have automatically detected it and you should proceed to the next section, Install TCP/IP. Optionally, you may follow steps 1-3 below to confirm that your card is recognized.

If you obtained an Ethernet interface after Windows 95/98/Me was already on your computer, then do the following:

STEP 1: From the Start menu, select Settings and then select Control Panel.

STEP 2: Double-click on the System icon, then click on the tab labeled Device Manager.

STEP 3: Double-click on Network adapters to display a list of the network interfaces that are installed on your computer. If you see two entries other than the Dial-Up Adapter, one is your second Ethernet card. Skip ahead to Install TCP/IP. If you do not see your second Ethernet card, continue to step 4 to install it.



STEP 4: If an entry for your second Ethernet card appears here, you probably do not need to run any software included with your card, but keep the software handy just in case you need it later to resolve a problem.

STEP 5: Note the name of your second Ethernet card.

STEP 6: Close the System Properties window (the Control Panel window should still be open).

STEP 7: Open the Add New Hardware control panel and follow the on-screen instructions. We recommend that you allow Windows to search for and install your card automatically.

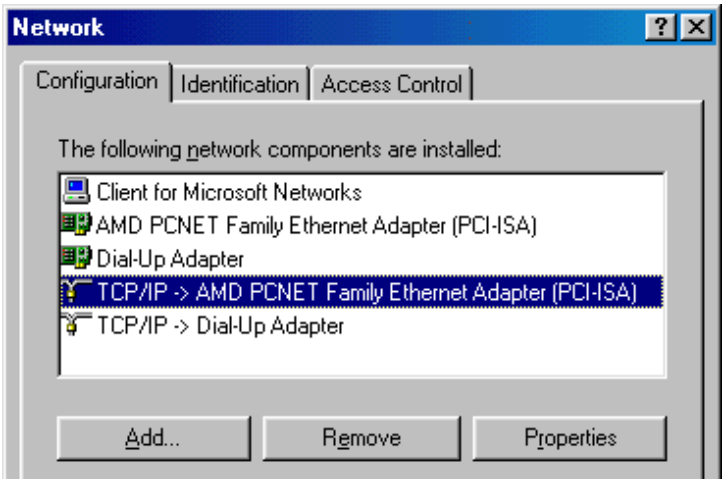
STEP 8: Restart your computer if Windows gives you the option to do so. Then continue with Install TCP/IP.

Install TCP/IP

To determine whether TCP/IP software is already installed on your computer, follow these steps:

STEP 1: From the Start menu, select Settings and then Control Panel.

STEP 2: Double-click on the Network icon. Click on the Configuration tab if it is not already selected.



STEP 3: Look in the box labeled The following network components are installed.

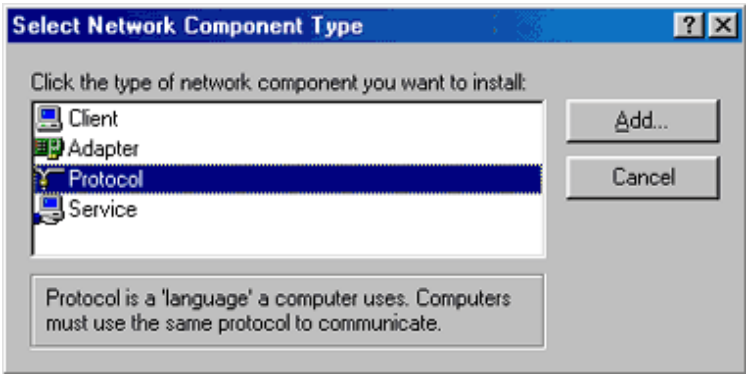
STEP 4: If you see IPX/SPX-compatible Protocol or NetBEUI in the list, select it, then click the Remove button to delete it. These protocols are used by some networked applications, especially games, but they may interfere with your Ethernet connection.

STEP 5: If you don't see TCP/IP for your second Ethernet card, ~~then~~ continue with step 4.
If you do see TCP/IP for your second Ethernet card, skip ahead to Configure TCP/IP.

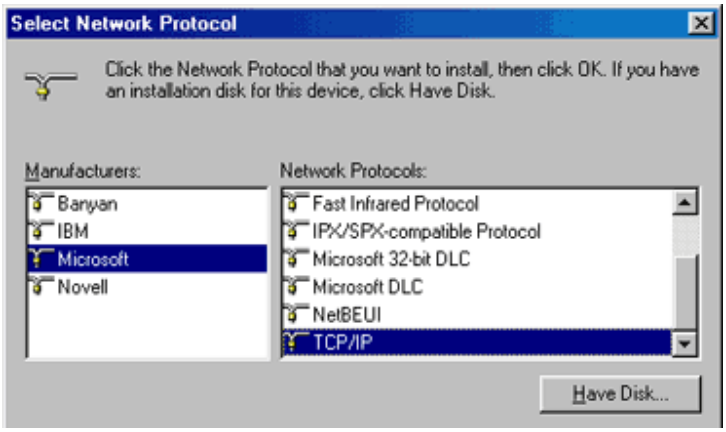
Do these steps only if you do not see TCP/IP listed in your Network control panel for your second Ethernet card.

STEP 6: In the Network control panel, click the Add... button.

STEP 7: In the Select Network Component Type window, choose Protocol and click the Add... button.



STEP 8: In the Select Network Protocol window, select Microsoft under Manufacturer and TCP/IP under Network Protocols.



STEP 9: Click the OK button to return to the Network control panel, then click the OK button again to exit the control panel.

STEP 10: Restart your computer if Windows gives you the option to do so. Then continue with Configure TCP/IP.

Configure TCP/IP

STEP 1: From the Start menu, select Settings and then Control Panel. Double-click on the Network icon. Click the Configuration tab if it is not already selected.

STEP 2: In the box labeled The following network components are installed, select TCP/IP. TCP/IP is listed at least twice, so choose the one followed by the name of your second Ethernet card (do not choose TCP/IP -> Dial-up Adapter).

STEP 3: Click the Properties button.

STEP 4: In the TCP/IP Properties window, click on the IP Address tab.

STEP 5: Make sure that Specify an IP address is selected.

STEP 6: Enter `192.168.100.1` for IP Address and `255.255.255.0` for Subnet Mask.

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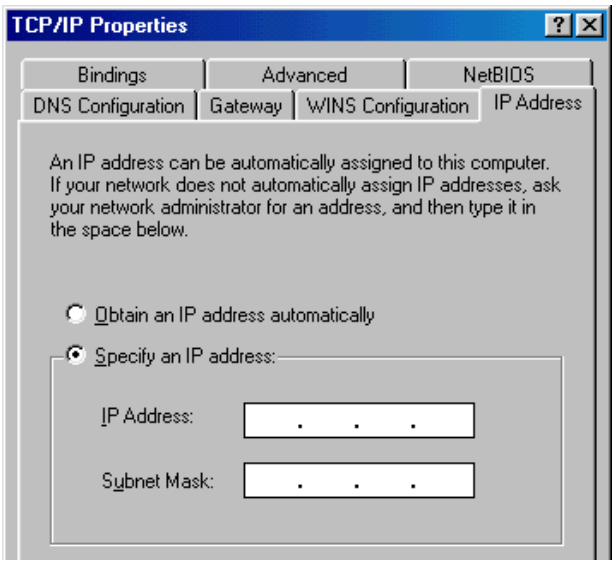
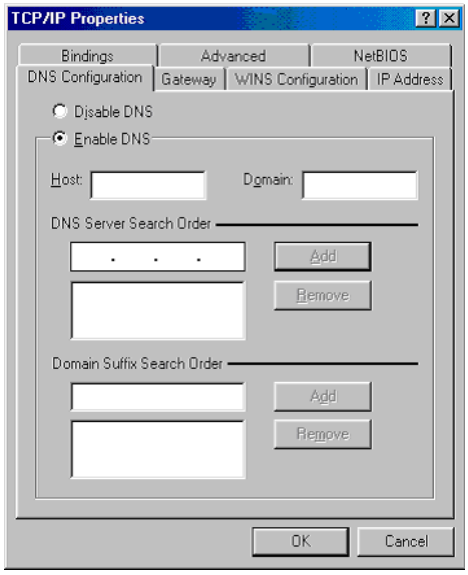

TCP/IP Properties
Bindings
Advanced
NetBIOS
DNS Configuration
Gateway
WINS Configuration
IP Address
An IP address can be automatically assigned to this computer. If your network does not automatically assign IP addresses, ask your network administrator for an address, and then type it in the space below.
Obtain an IP address automatically
Specify an IP address:
IP Address:
Subnet Mask:

STEP 7: Click on the DNS Configuration tab.

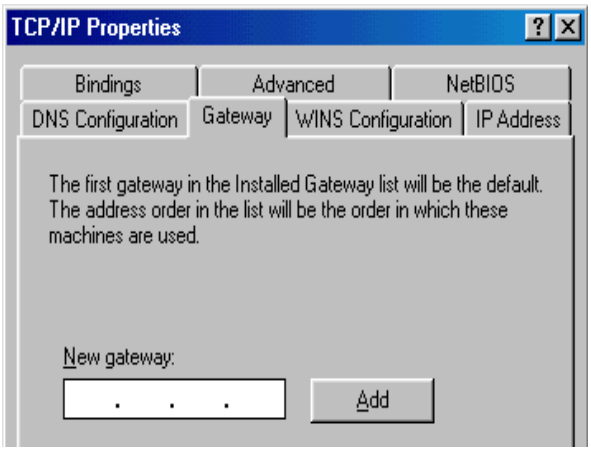
STEP 8: Select Enable DNS.

Make sure the Host and Domain information is blank.



STEP 9: Click on the Gateway tab.

Make sure the box labeled New gateway is blank.



STEP 10: Click the OK button to return to the Network control panel.

STEP 11: Click OK to exit the Network control panel.

STEP 12: Restart your computer if Windows gives you the option to do so.

Appendix B

Field Replacement of Fuses on DNA and DNR Boards

Some boards used in UEI DAQ I/O systems require field replacement of fuses when unexpected overloads occur. Locations of these fuses are shown in **Figure 9-1** through **Figure 9-3**. Part numbers for the replacement fuses are listed **Table B-1**.

Table B-1. DNA/DNR Replacement Fuses

UEI Fuse ID (Board)	Rating	UEI Part No.	Description	Mfr.	Mfr P/N
F1	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F2	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F3 (DC)	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR
F3 (1GB)	10A	925-1125	FUSE 10A 125V FAST NAN02 SMD	Littlefuse	0451010.MRL
F4	5A	925-5125	FUSE 5A 125V SLO SMD SILVER T/R	Littlefuse	0454005.MR

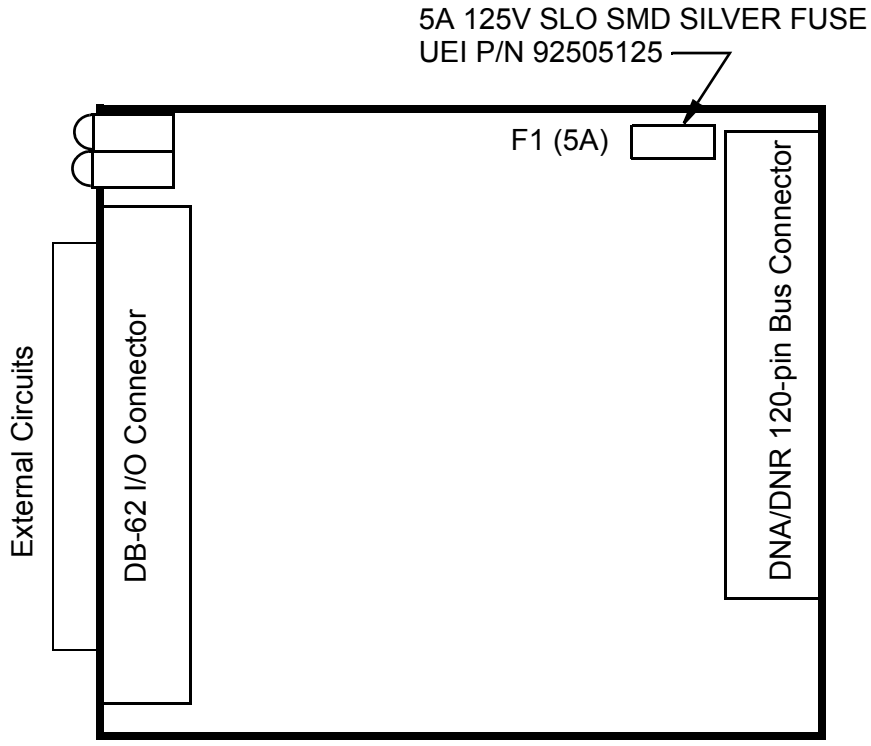


Figure 9-1. Location of Fuse for PL-61x, PL-62x, and PL-63x Boards

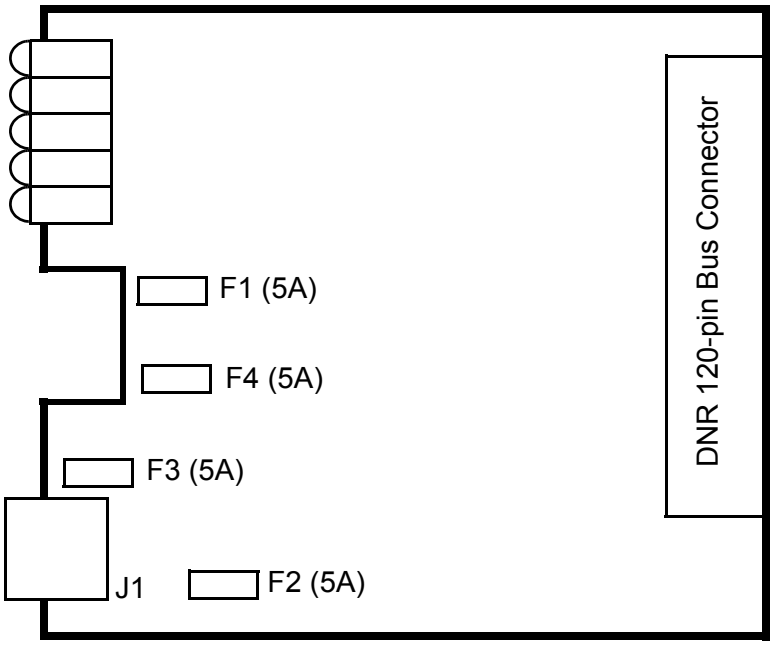


Figure 9-2. Location of Fuses for DNR-POWER-DC Board

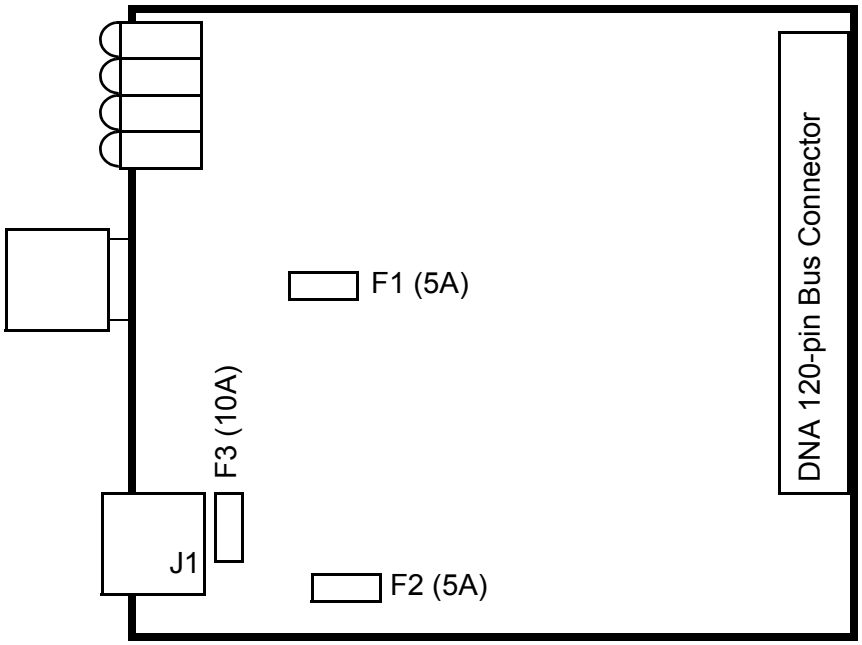


Figure 9-3. Location of Fuses for DNR-POWER-1GB Board

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